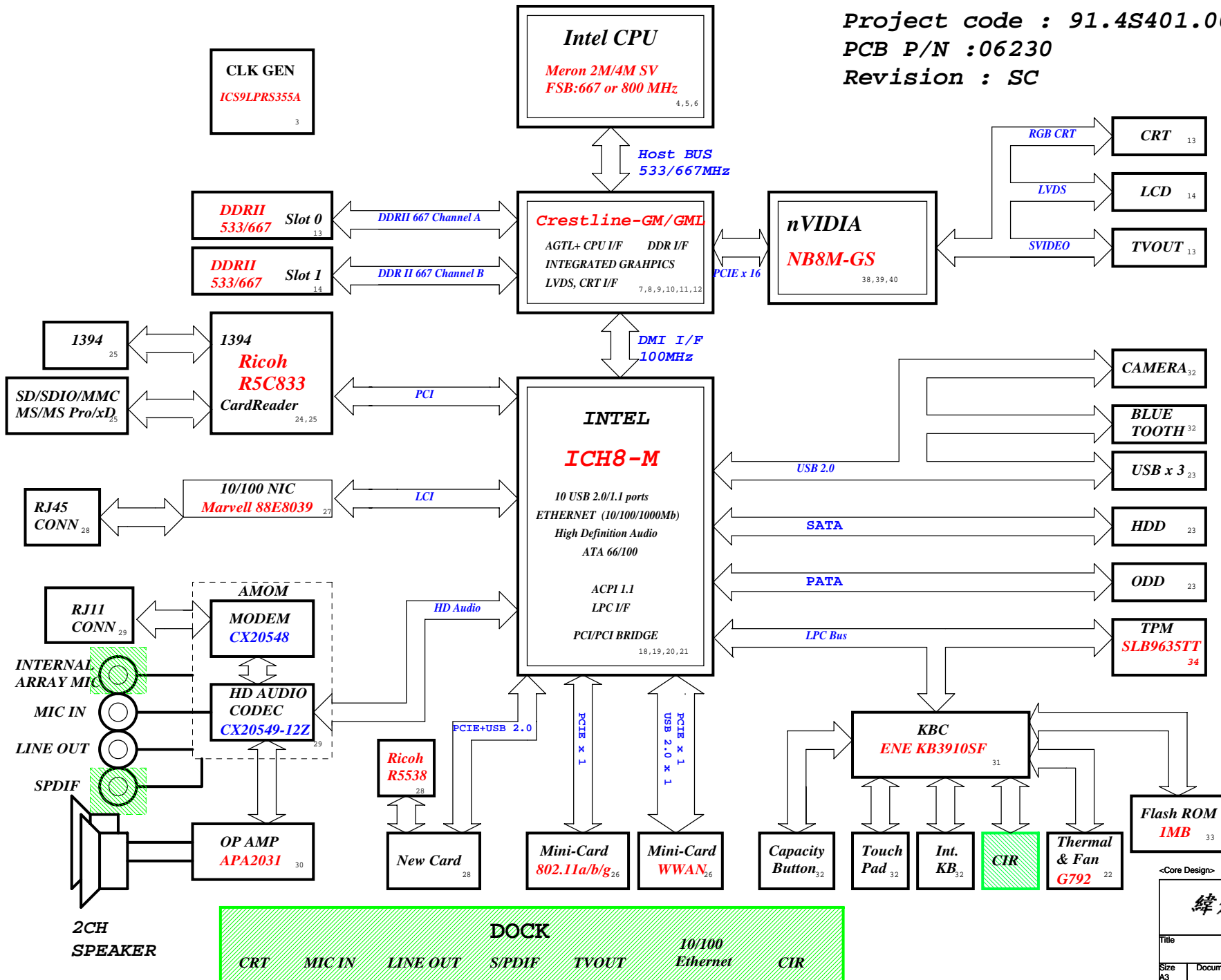


Pamirs-Discrete Block Diagram

Project code : 91.4S401.001
PCB P/N :06230
Revision : SC



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_s3 3V_s5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_s0 1D8V_s3
SYSTEM DC/DC FAN5234	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_s0 11A
MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA
CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A
PCB LAYER	
L1: Signal 1	
L2: GND	
L3: Signal 2	
L4: Signal 3	
L5: GND	
L6: VCC	
L7: Signal 4	
L8: Signal 5	
L9: GND	
L10: Signal 5	

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVP_Tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIe port cofig bit1

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

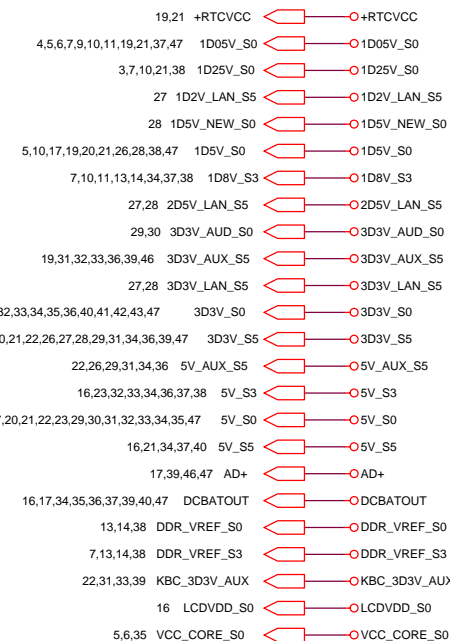
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

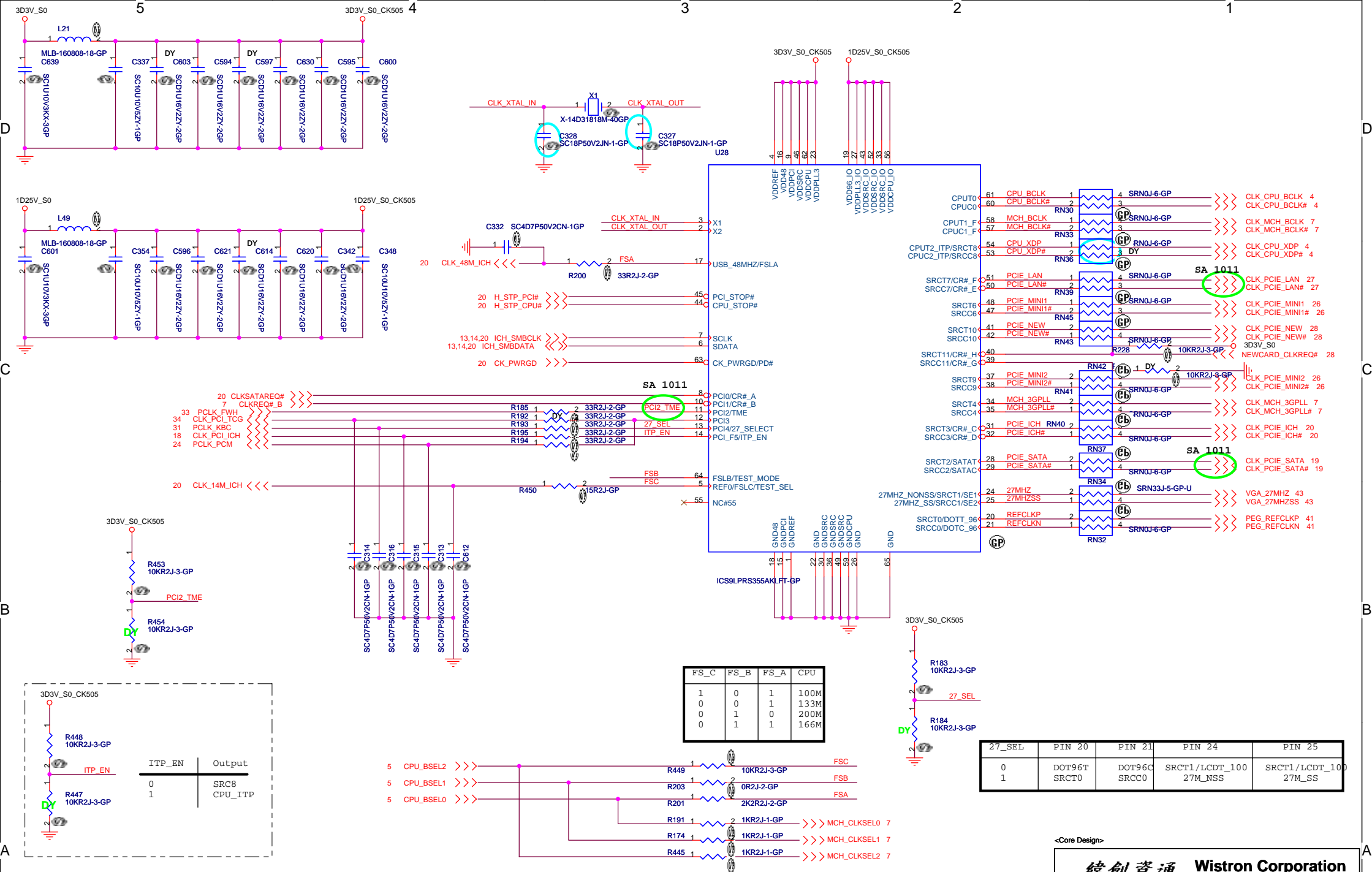
SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD



INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 8	Low Power PCI Express	Low Power mode
CFG 9	PCI Express Graphics Lane Reversal	Normal Mode(Lanes number in order)
CFG 16	FSB Dynamic ODT	Disabled
CFG 19	DMI Lane Reserved	Reserved Lane
CFG 20	Concurrent SDVO/PCIe	Only PCIe or SDVO is operation
SDVO_CTRL_DATA	NO SDVO Card Present	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13	Reserved	
LL(00)	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
NH(11)	Normal Operation	

<Core Design>		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Table of Content		
Size A3	Document Number	Rev
Pamirs-Discrete		SA
Date: Wednesday, November 01, 2006 Sheet 2 of 47		



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Clock generator CY28548

Size
A3

Document Number

Pamirs-Discrete

Rev
SC

Date: Tuesday, December 19, 2006

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7 H_D#0[0.63] <<>>

7 H_DSTBN#0 <<>>
7 H_DSTBP#0 <<>>
7 H_DINV#0 <<>>

7 H_DSTBN#1 <<>>
7 H_DSTBP#1 <<>>
7 H_DINV#1 <<>>

V_CPU_GTLREF

TPAD28 TP19

TPAD28 TP22

TPAD28 TP26

TPAD28 TP3

TPAD28 TP21

TEST1 C23

TEST2 D25

TEST3 C24

TEST4 AF26

TEST5 AE1

TEST6 A26

B22

B23

B21

C21

BSEL0

BSEL1

BSEL2

CPU_BSEL0

CPU_BSEL1

CPU_BSEL2

3 CPU_BSEL0

3 CPU_BSEL1

3 CPU_BSEL2

SCD1U16V2KX-3GP

C296

1

DY

PLACE C173 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals

CPU_BSEL

CPU_BSEL2

CPU_BSEL1

CPU_BSEL0

166

0

1

1

200

0

Close to CPU pin AD26

Z0=55 ohm

with in

500mils .

1905V_S0

R422

1KR2F-3-GP

V_CPU_GTLREF

R423

2KR2F-3-GP

C602

SCD0U16V2KX-3GP

U62B 2 OF 4

H_D#0 F22C

H_D#1 F24C

H_D#2 E26C

H_D#3 G22C

H_D#4 F23C

H_D#5 G25C

H_D#6 E25C

H_D#7 F23C

H_D#8 K24C

H_D#9 G24C

H_D#10 J24C

H_D#11 J23C

H_D#12 H22C

H_D#13 F26C

H_D#14 K14C

H_D#15 H23C

H_D#16 N22C

H_D#17 K25C

H_D#18 P26C

H_D#19 R23C

H_D#20 L23C

H_D#21 M24C

H_D#22 L22C

H_D#23 M23C

H_D#24 P25C

H_D#25 P23C

H_D#26 P22C

H_D#27 T24C

H_D#28 R24C

H_D#29 L25C

H_D#30 T25C

H_D#31 N25C

H_D#32 D0#

H_D#33 D1#

H_D#34 D2#

H_D#35 D3#

H_D#36 D4#

H_D#37 D5#

H_D#38 D6#

H_D#39 D7#

H_D#40 D8#

H_D#41 D9#

H_D#42 D10#

H_D#43 D11#

H_D#44 D12#

H_D#45 D13#

H_D#46 D14#

H_D#47 D15#

H_D#48 D16#

H_D#49 D17#

H_D#50 D18#

H_D#51 D19#

H_D#52 D20#

H_D#53 D21#

H_D#54 D22#

H_D#55 D23#

H_D#56 D24#

H_D#57 D25#

H_D#58 D26#

H_D#59 D27#

H_D#60 D28#

H_D#61 D29#

H_D#62 D30#

H_D#63 D31#

H_D#64 D32#

H_D#65 D33#

H_D#66 D34#

H_D#67 D35#

H_D#68 D36#

H_D#69 D37#

H_D#70 D38#

H_D#71 D39#

H_D#72 D40#

H_D#73 D41#

H_D#74 D42#

H_D#75 D43#

H_D#76 D44#

H_D#77 D45#

H_D#78 D46#

H_D#79 D47#

H_D#80 D48#

H_D#81 D49#

H_D#82 D50#

H_D#83 D51#

H_D#84 D52#

H_D#85 D53#

H_D#86 D54#

H_D#87 D55#

H_D#88 D56#

H_D#89 D57#

H_D#90 D58#

H_D#91 D59#

H_D#92 D60#

H_D#93 D61#

H_D#94 D62#

H_D#95 D63#

H_D#96 D64#

H_D#97 D65#

H_D#98 D66#

H_D#99 D67#

H_D#100 D68#

H_D#101 D69#

H_D#102 D70#

H_D#103 D71#

H_D#104 D72#

H_D#105 D73#

H_D#106 D74#

H_D#107 D75#

H_D#108 D76#

H_D#109 D77#

H_D#110 D78#

H_D#111 D79#

H_D#112 D80#

H_D#113 D81#

H_D#114 D82#

H_D#115 D83#

H_D#116 D84#

H_D#117 D85#

H_D#118 D86#

H_D#119 D87#

H_D#120 D88#

H_D#121 D89#

H_D#122 D90#

H_D#123 D91#

H_D#124 D92#

H_D#125 D93#

H_D#126 D94#

H_D#127 D95#

H_D#128 D96#

H_D#129 D97#

H_D#130 D98#

H_D#131 D99#

H_D#132 D100#

H_D#133 D101#

H_D#134 D102#

H_D#135 D103#

H_D#136 D104#

H_D#137 D105#

H_D#138 D106#

H_D#139 D107#

H_D#140 D108#

H_D#141 D109#

H_D#142 D110#

H_D#143 D111#

H_D#144 D112#

H_D#145 D113#

H_D#146 D114#

H_D#147 D115#

H_D#148 D116#

H_D#149 D117#

H_D#150 D118#

H_D#151 D119#

H_D#152 D120#

H_D#153 D121#

H_D#154 D122#

H_D#155 D123#

H_D#156 D124#

H_D#157 D125#

H_D#158 D126#

H_D#159 D127#

H_D#160 D128#

H_D#161 D129#

H_D#162 D130#

H_D#163 D131#

H_D#164 D132#

H_D#165 D133#

H_D#166 D134#

H_D#167 D135#

H_D#168 D136#

H_D#169 D137#

H_D#170 D138#

H_D#171 D139#

H_D#172 D140#

H_D#173 D141#

H_D#174 D142#

H_D#175 D143#

H_D#176 D144#

H_D#177 D145#

H_D#178 D146#

H_D#179 D147#

H_D#180 D148#

H_D#181 D149#

H_D#182 D150#

H_D#183 D151#

H_D#184 D152#

H_D#185 D153#

H_D#186 D154#

H_D#187 D155#

H_D#188 D156#

H_D#189 D157#

H_D#190 D158#

H_D#191 D159#

H_D#192 D160#

H_D#193 D161#

H_D#194 D162#

H_D#195 D163#

H_D#196 D164#

H_D#197 D165#

H_D#198 D166#

H_D#199 D167#

H_D#200 D168#

H_D#201 D169#

H_D#202 D170#

H_D#203 D171#

H_D#204 D172#

H_D#205 D173#

H_D#206 D174#

H_D#207 D175#

H_D#208 D176#

H_D#209 D177#

H_D#210 D178#

H_D#211 D179#

H_D#212 D180#

H_D#213 D181#

H_D#214 D182#

H_D#215 D183#

H_D#216 D184#

H_D#217 D185#

H_D#218 D186#

H_D#219 D187#

H_D#220 D188#

H_D#221 D189#

H_D#222 D190#

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H_D#226 D194#

H_D#227 D195#

H_D#228 D196#

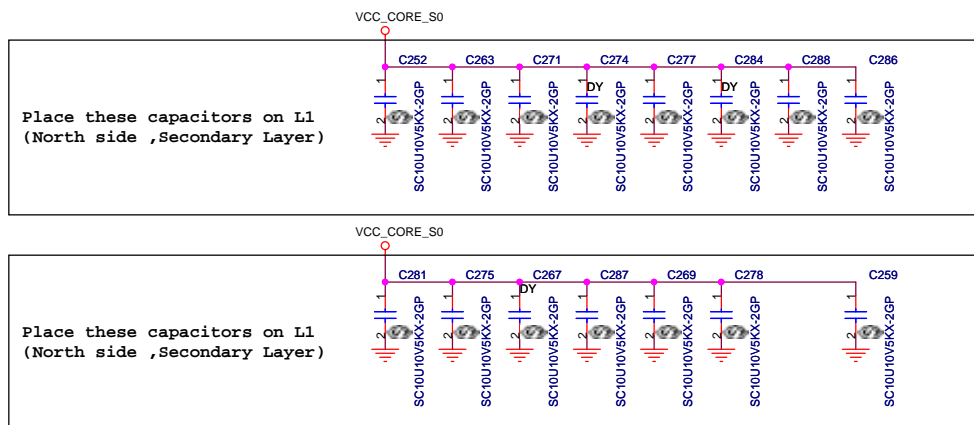
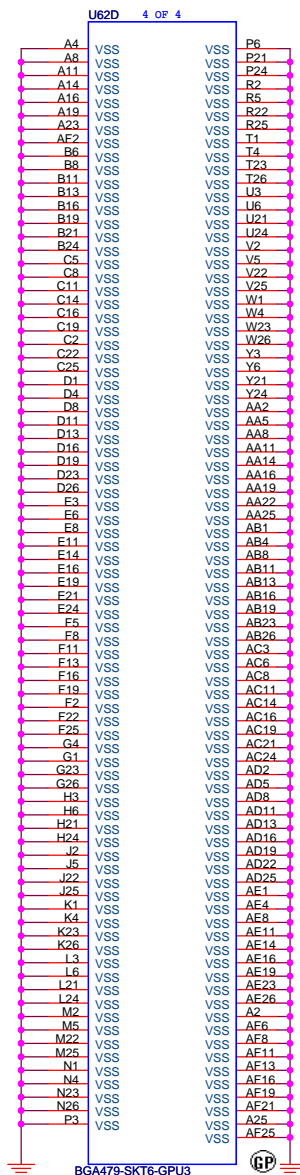
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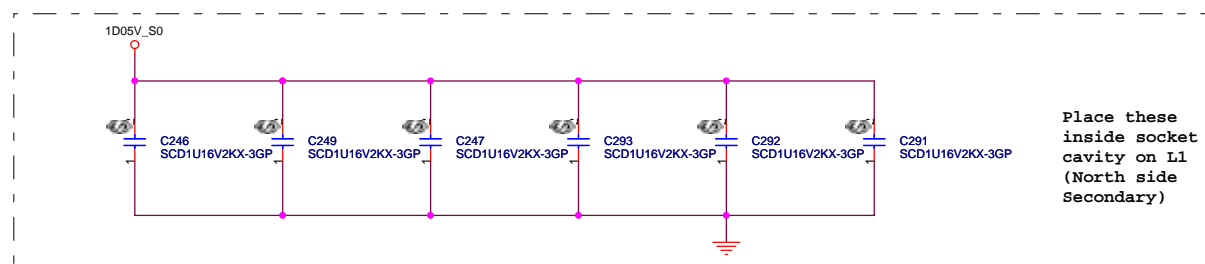
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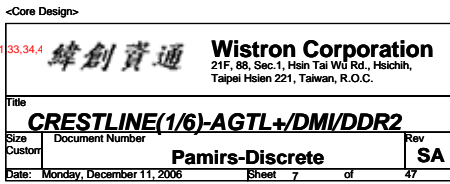
H_D#233 D201#



Mid Frequncd Decoupling



<Core Design>



D

C

B

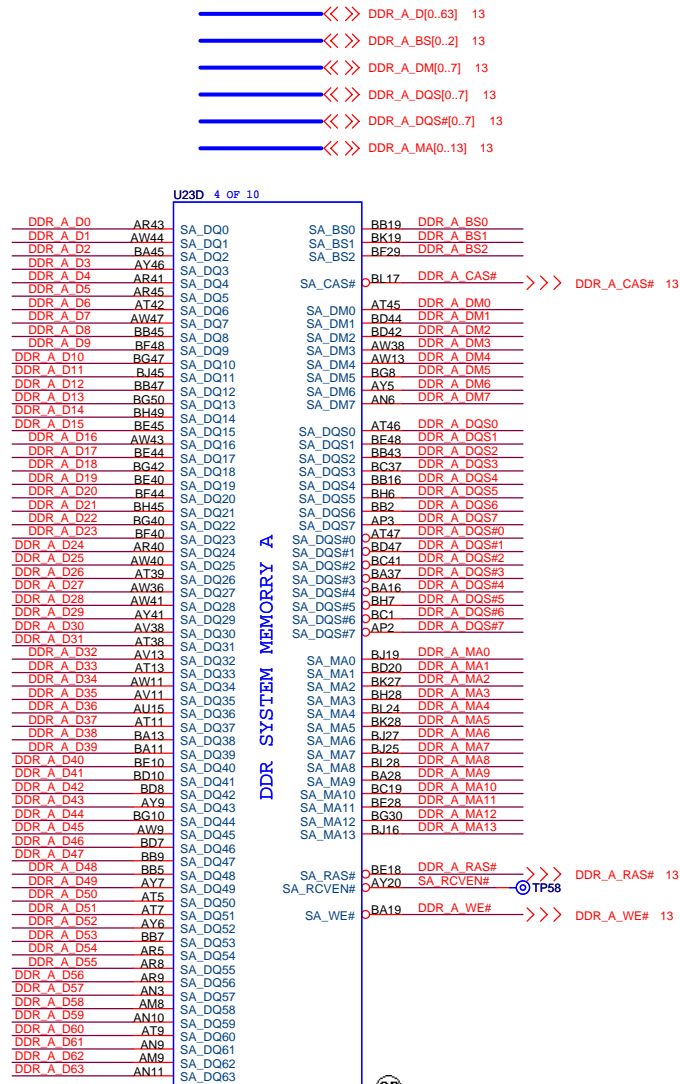
A

D

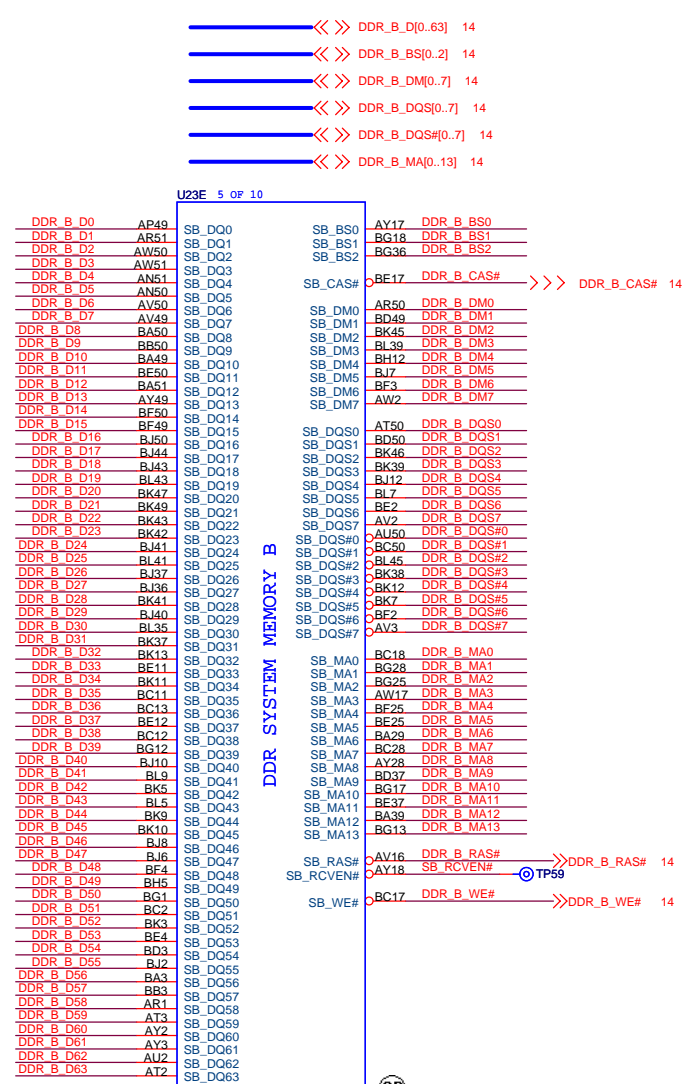
C

B

A



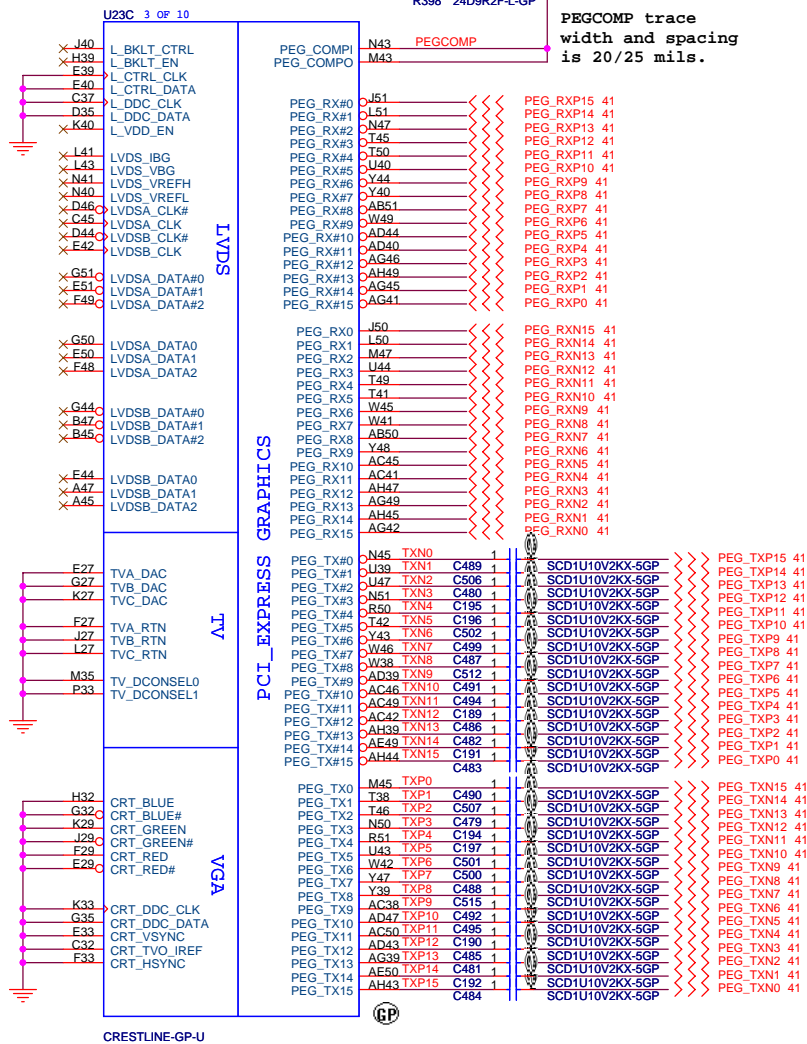
CRESTLINE-GP-U



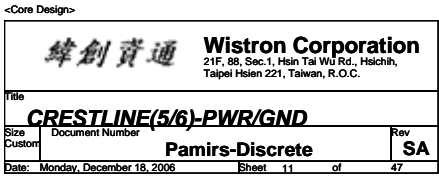
CRESTLINE-GP-U

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
CRESTLINE(2/6)-DDR2 A/B CH		
Size	Document Number	Rev
A3		SA
Date: Wednesday, October 18, 2006		
Sheet 8 of 47		



Strap Pin Table	
CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.



U23I 9 OF 10

A13	VSS	AW24
A15	VSS	AW29
A17	VSS	AW32
A24	VSS	AW5
AA21	VSS	AW7
AA24	VSS	AY10
AA29	VSS	AY24
AB20	VSS	AY37
AB23	VSS	AY42
AB26	VSS	AY43
AB28	VSS	AY45
AB31	VSS	AY47
AC10	VSS	AY50
AC13	VSS	B10
AC3	VSS	B20
AC39	VSS	B24
AC43	VSS	B29
AC47	VSS	B30
AD1	VSS	B35
AD21	VSS	B38
AD26	VSS	B43
AD29	VSS	B46
AD3	VSS	B5
AD41	VSS	B8
AD45	VSS	BA1
AD49	VSS	BA17
AD5	VSS	BA18
AD50	VSS	BA2
AD8	VSS	BA24
AE10	VSS	BB12
AE14	VSS	BB25
AE6	VSS	BB40
AE20	VSS	BB44
AE23	VSS	BB49
AE24	VSS	BB8
AF31	VSS	BC16
AG2	VSS	BC24
AG38	VSS	BC25
AG43	VSS	BC38
AG47	VSS	BC40
AG50	VSS	BC51
AH3	VSS	BD13
AH40	VSS	BD2
AH41	VSS	BD28
AH7	VSS	BD45
AH9	VSS	BD48
AJ11	VSS	BD5
AJ13	VSS	BE1
AJ21	VSS	BE19
AJ24	VSS	BE23
AJ29	VSS	BE30
AJ32	VSS	BE42
AJ43	VSS	BE51
AJ45	VSS	BE8
AJ49	VSS	BF12
AK20	VSS	BF16
AK21	VSS	BF36
AK26	VSS	BG19
AK28	VSS	BG2
AK31	VSS	BG24
AK51	VSS	BG29
AL1	VSS	BG39
AM11	VSS	BG48
AM13	VSS	BG5
AM3	VSS	BG51
AM4	VSS	BH17
AM41	VSS	BH30
AM45	VSS	BH44
AN1	VSS	BH46
AN38	VSS	BH8
AN39	VSS	BJ11
AN43	VSS	BJ13
AN5	VSS	BJ38
AN7	VSS	BJ4
AP4	VSS	BJ42
AP48	VSS	BJ46
AP50	VSS	BK15
AR11	VSS	BK17
AR2	VSS	BK25
AR39	VSS	BK29
AR44	VSS	BK36
AR47	VSS	BK40
AR7	VSS	BK44
AT10	VSS	BK6
AT14	VSS	BK8
AT41	VSS	BL11
AT49	VSS	BL13
AU1	VSS	BL19
AU23	VSS	BL22
AU29	VSS	BL37
AU3	VSS	BL47
AU36	VSS	C12
AU49	VSS	C16
AU51	VSS	C19
AV39	VSS	C28
AV48	VSS	C29
AW1	VSS	C33
AW12	VSS	C36
AW16	VSS	C41

CRESTLINE-GP-U

U23J 10 OF 10

C46	VSS	W11
C50	VSS	W39
C7	VSS	W43
D13	VSS	W47
D24	VSS	W5
D3	VSS	W7
D32	VSS	Y13
D39	VSS	Y2
D45	VSS	Y41
D49	VSS	Y45
E10	VSS	Y49
E16	VSS	Y5
E24	VSS	Y50
E28	VSS	Y11
E32	VSS	P29
E47	VSS	T29
F19	VSS	T31
F36	VSS	T33
F4	VSS	R28
F40	VSS	
F50	VSS	
G1	VSS	
G13	VSS	
G16	VSS	AA32
G19	VSS	AB32
G24	VSS	AD32
G28	VSS	AE28
G29	VSS	AF29
G33	VSS	AT27
G42	VSS	AV25
G45	VSS	H50
G48	VSS	
GB44	VSS	
H24	VSS	
H28	VSS	
H4	VSS	
H45	VSS	
J11	VSS	
J16	VSS	
J2	VSS	
J24	VSS	
J28	VSS	
J33	VSS	
J35	VSS	
J39	VSS	
K12	VSS	
K47	VSS	
K8	VSS	
L1	VSS	
L17	VSS	
L20	VSS	
L24	VSS	
L28	VSS	
L3	VSS	
L33	VSS	
L49	VSS	
M28	VSS	
M42	VSS	
M46	VSS	
M49	VSS	
M5	VSS	
M50	VSS	
M9	VSS	
N11	VSS	
N14	VSS	
N17	VSS	
N29	VSS	
N32	VSS	
N36	VSS	
N39	VSS	
N44	VSS	
N49	VSS	
N7	VSS	
P19	VSS	
P2	VSS	
P23	VSS	
P3	VSS	
P50	VSS	
R49	VSS	
T39	VSS	
T43	VSS	
T47	VSS	
U41	VSS	
U45	VSS	
U50	VSS	
V2	VSS	
V3	VSS	

VSS

CRESTLINE-GP-U



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRESTLINE(6/6)-PWR/GND

Size

A3

Document Number

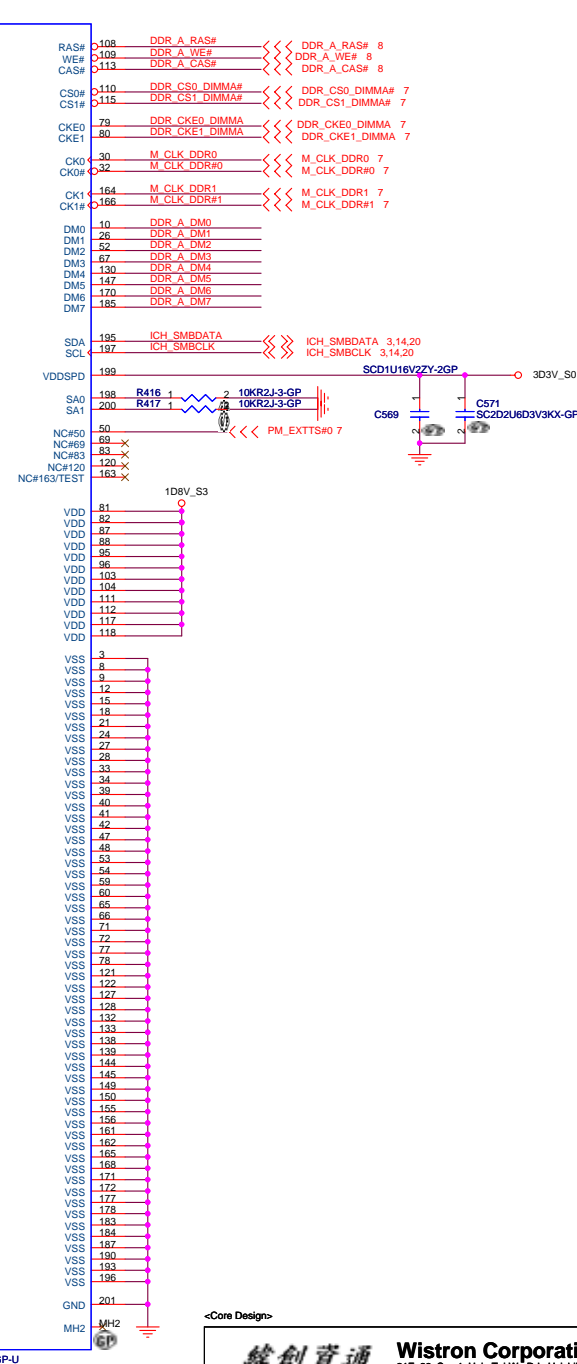
Pamirs-Discrete

Rev

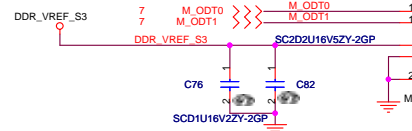
SA

Date: Wednesday, October 18, 2006

Sheet 12 of 47

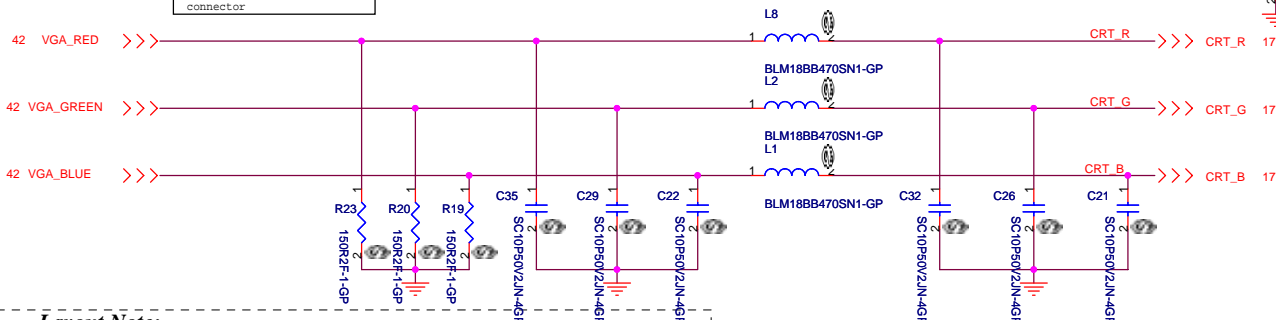


Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"



CRT I/F & CONNECTOR

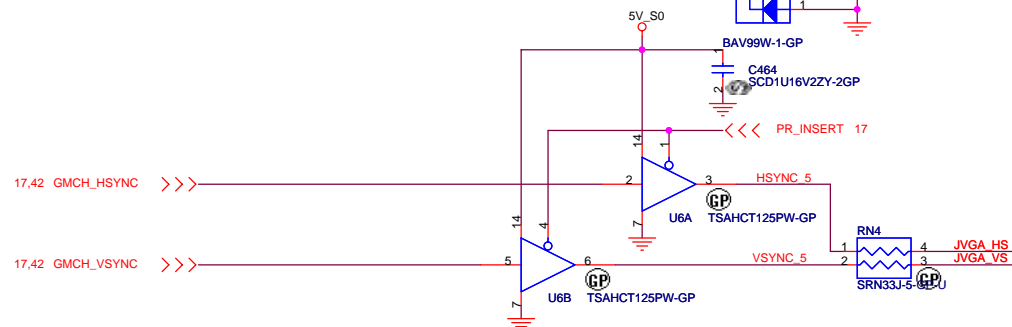
Layout Note:
Place these resistors
close to the CRT-out
connector



Layout Note:

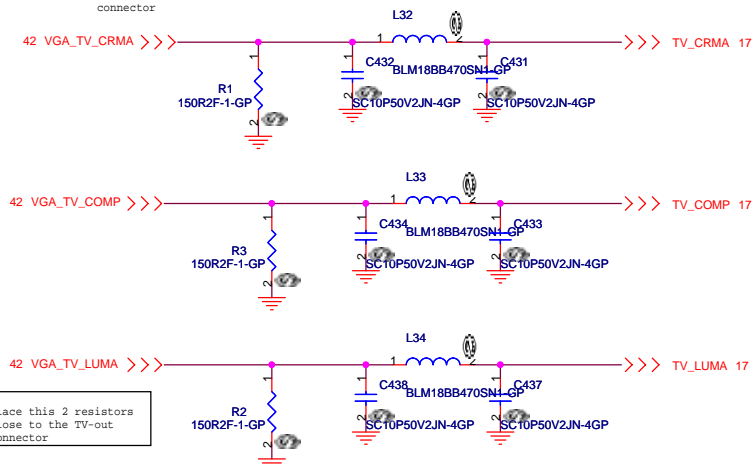
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

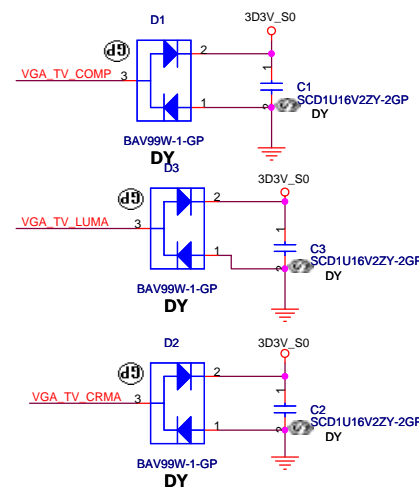
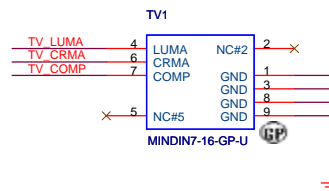


TV OUT CONN

connector



Place this 2 resistors
close to the TV-out
connector



<Core Design>

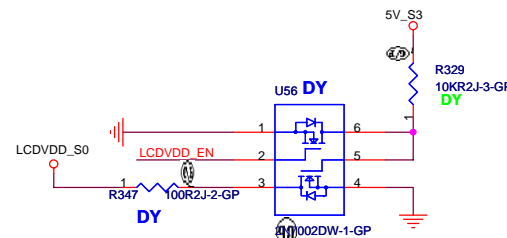
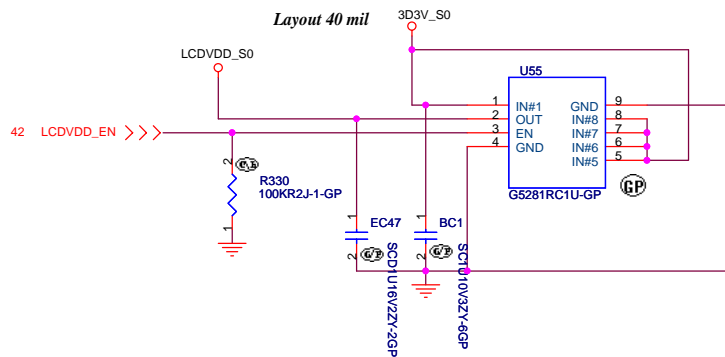
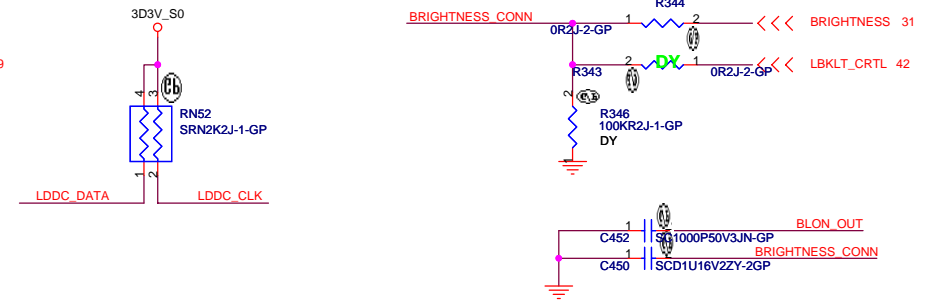
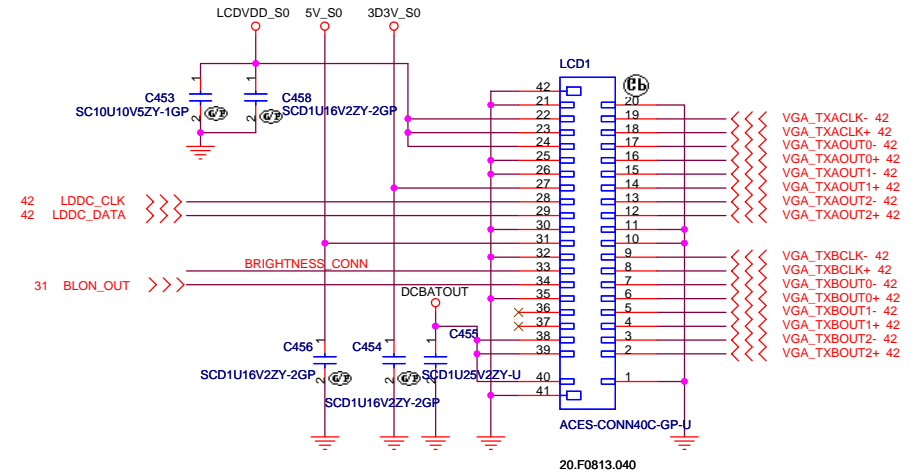
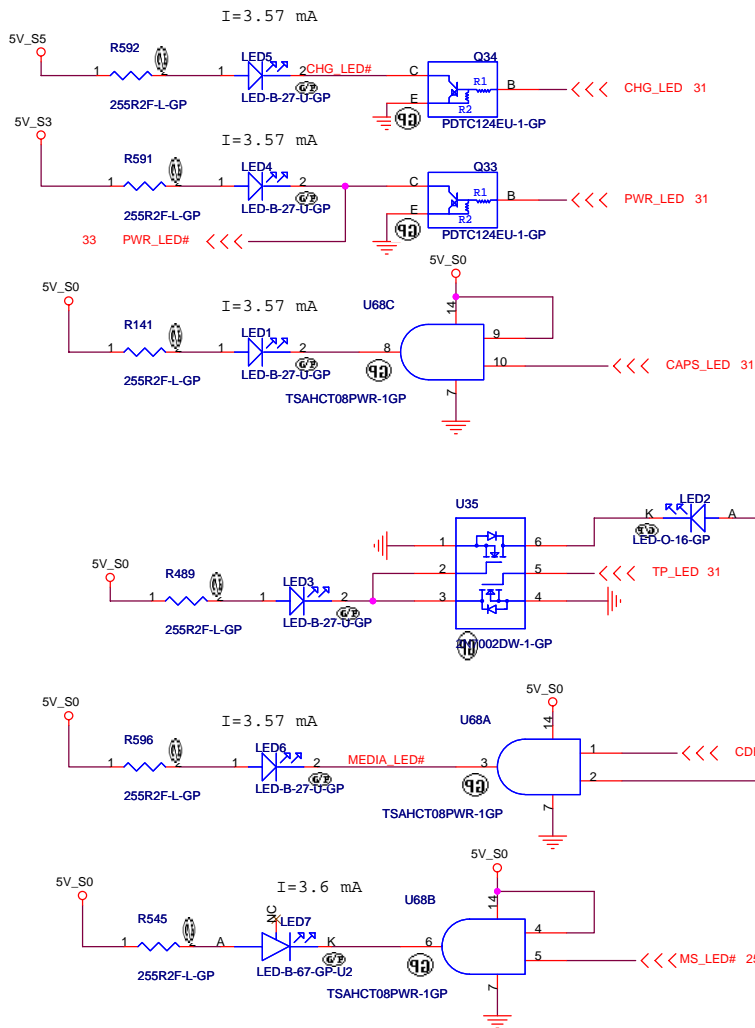
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CRT/TV Connector		
Size A3	Document Number	Rev SA
Date: Friday, November 24, 2006	Sheet 15 of 47	

LED / INVERTER INTERFACE

LCD/INV CONN



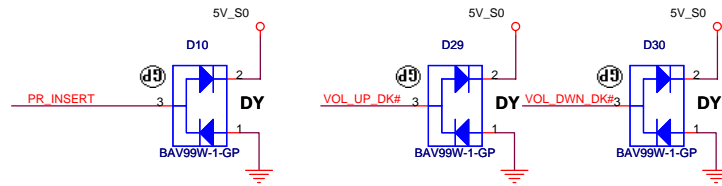
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緯創資通

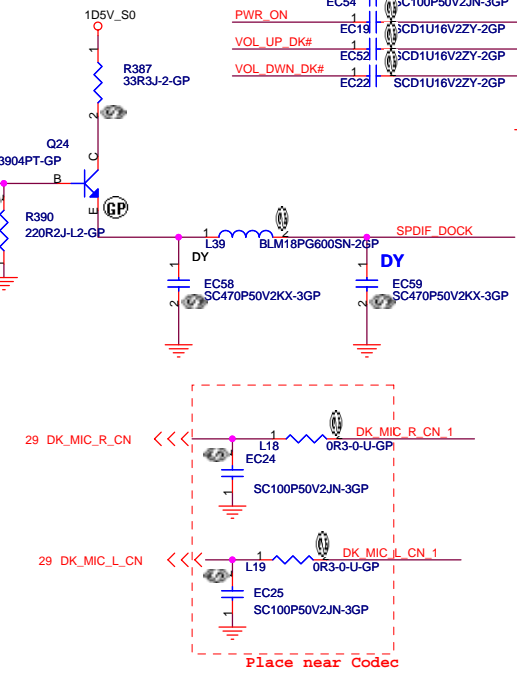
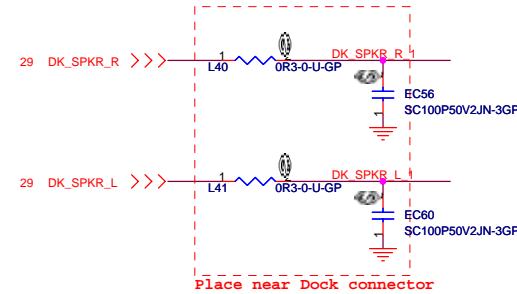
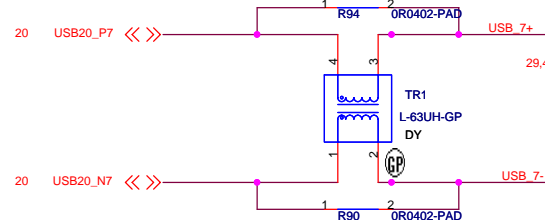
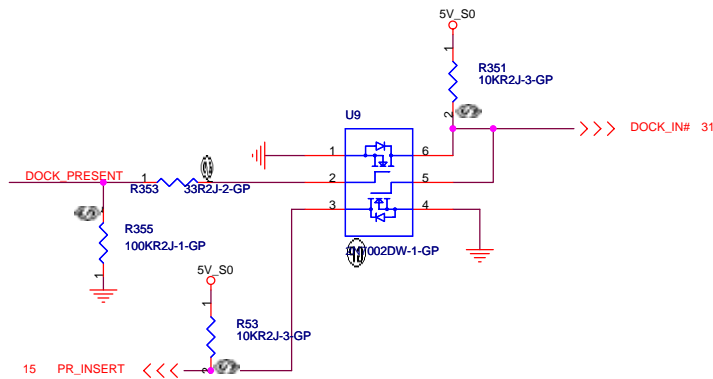
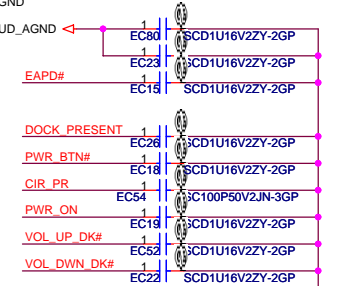
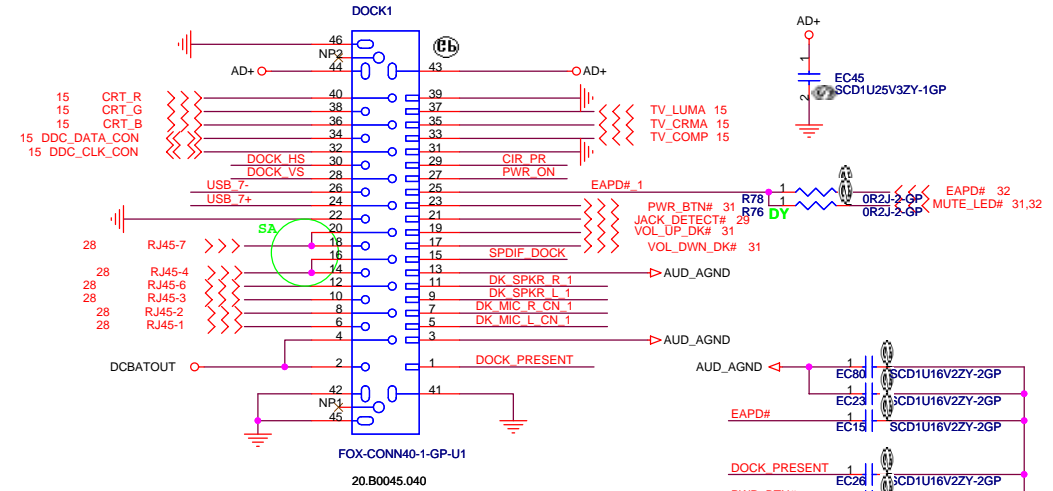
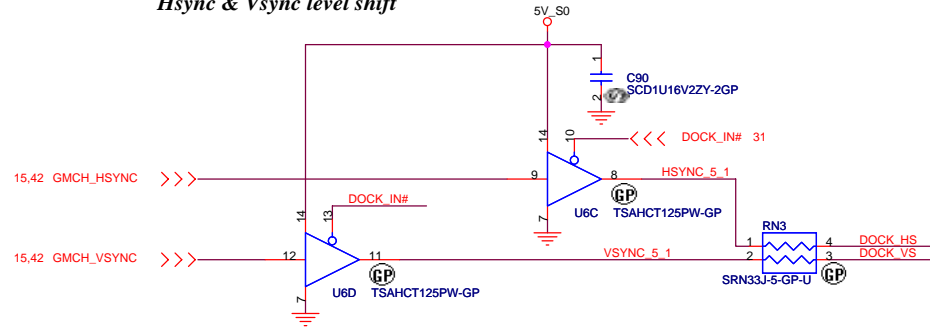
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

LCD/Inverter Connector			
Title	Document Number	Rev	SA
Size	Custom	Pamirs-Discrete	SA
Date: Tuesday, December 19, 2006	Sheet 16	of 47	

Docking Connector



Hsync & Vsync level shift

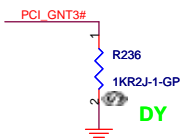
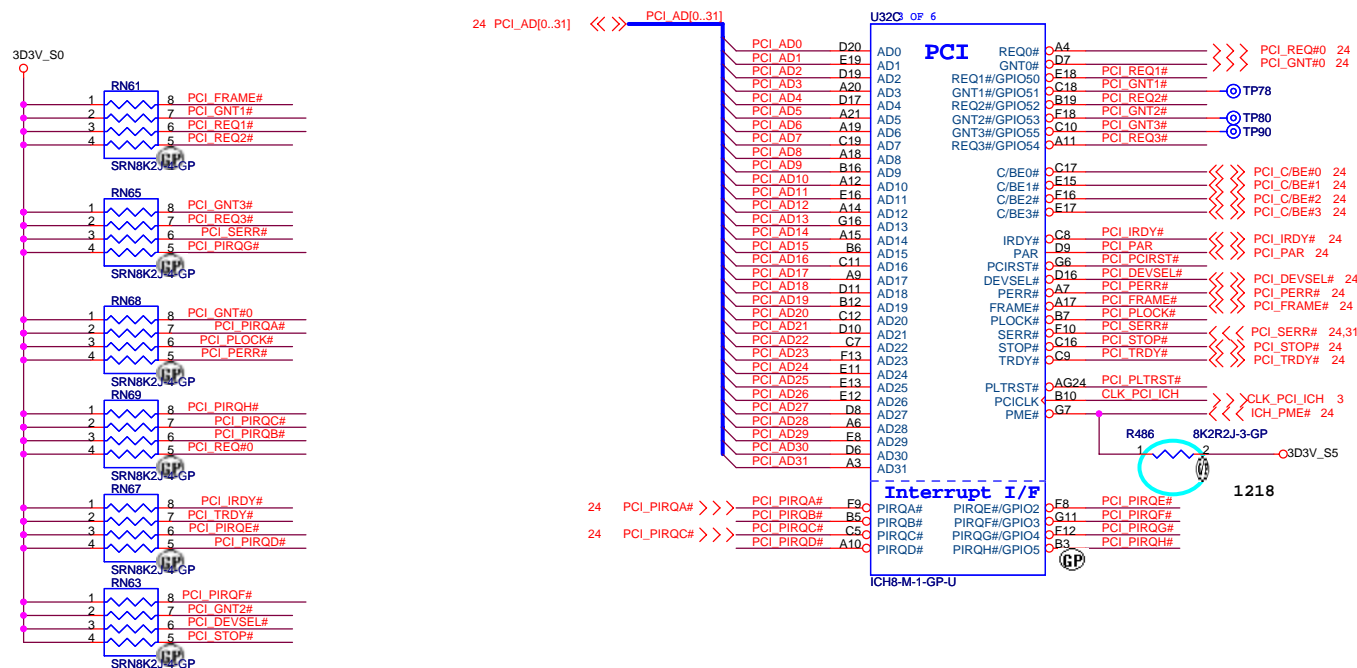


S0 = 4V
S3 = 2.5V
S5 = 0V

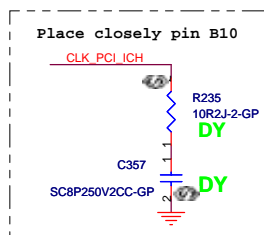
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

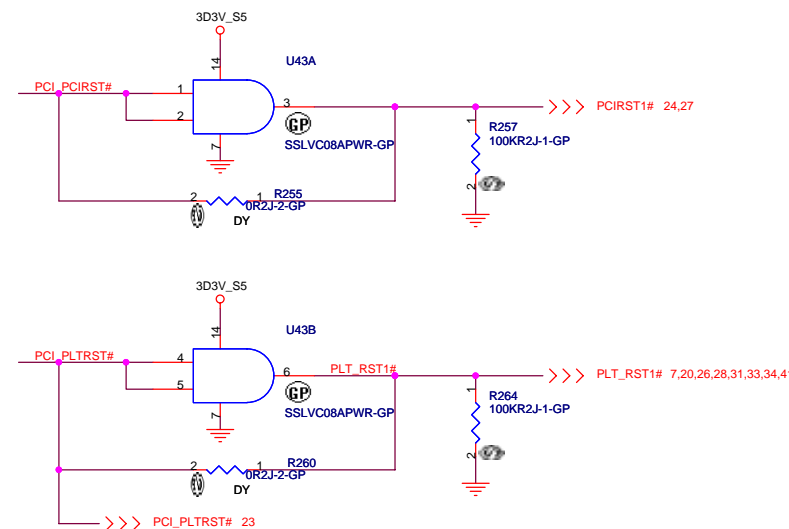
Title			Board to board conn/ Docking	
Size	Document Number			Rev
A3			Pamirs-Discrete	SA
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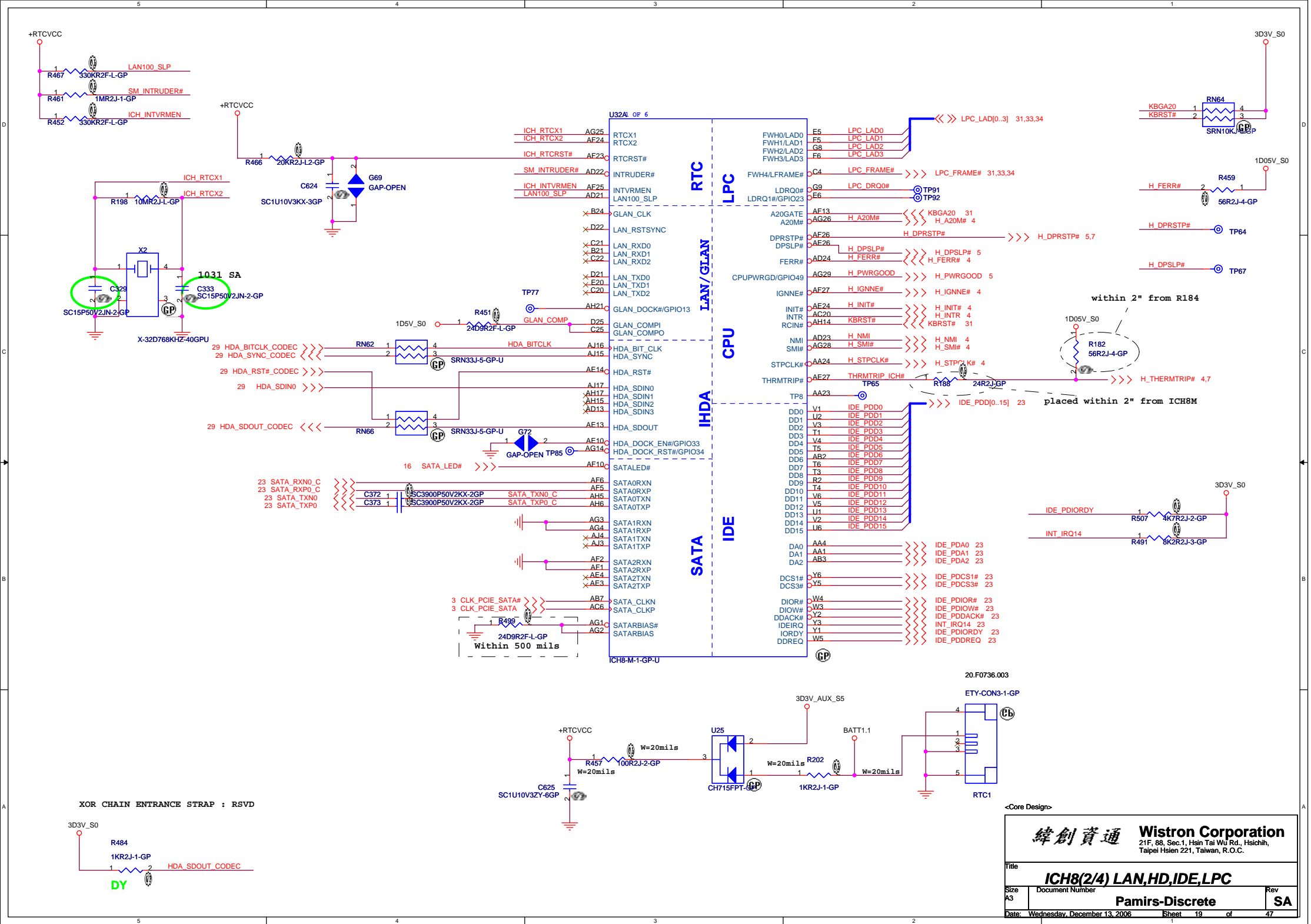
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

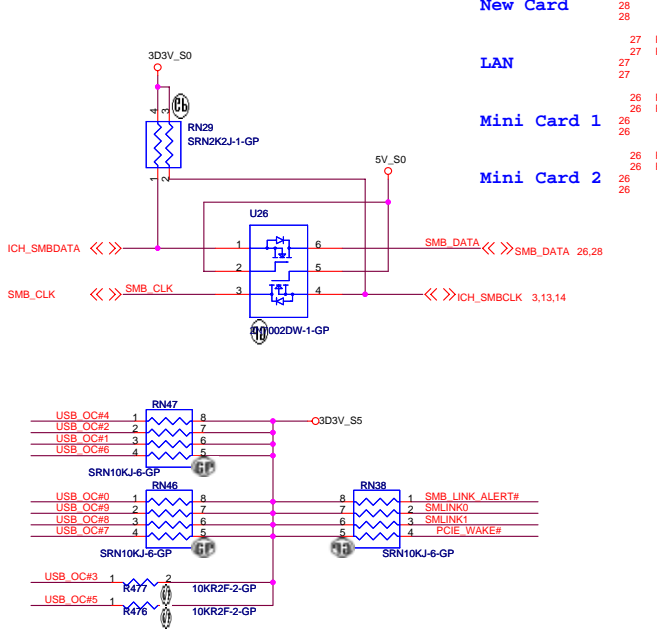
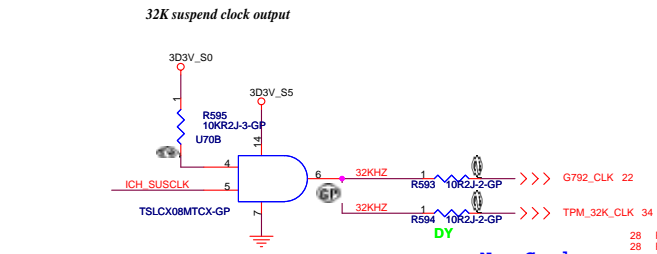
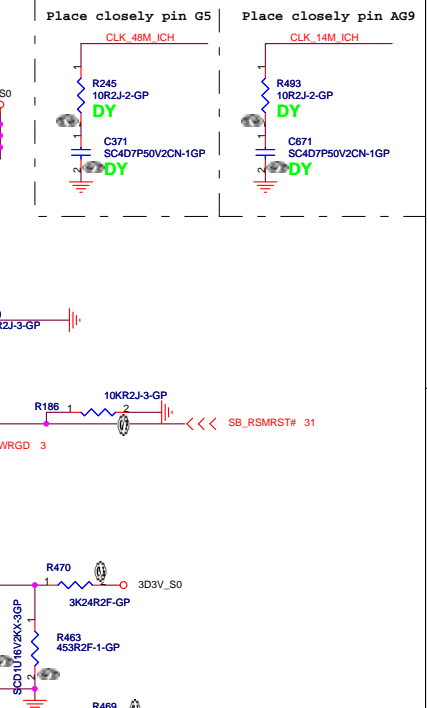
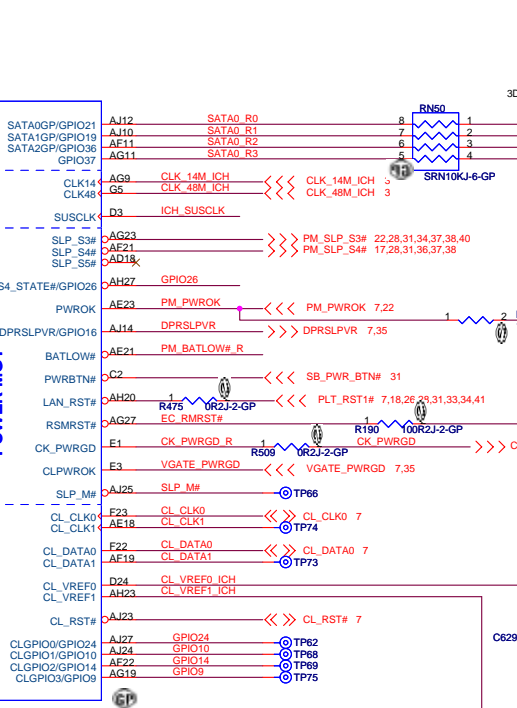
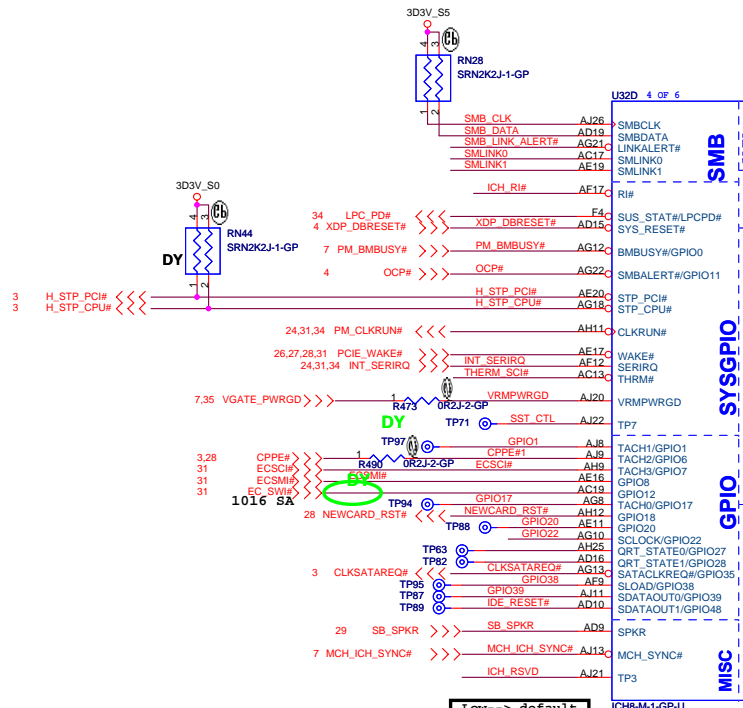
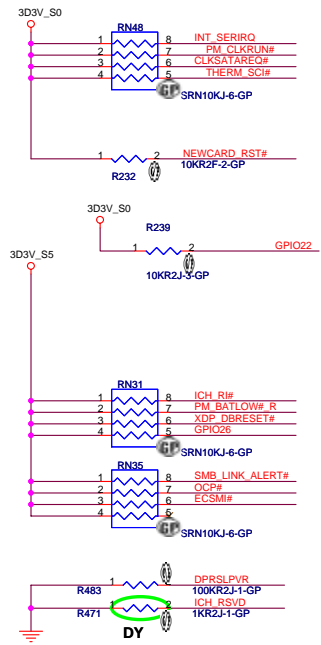


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



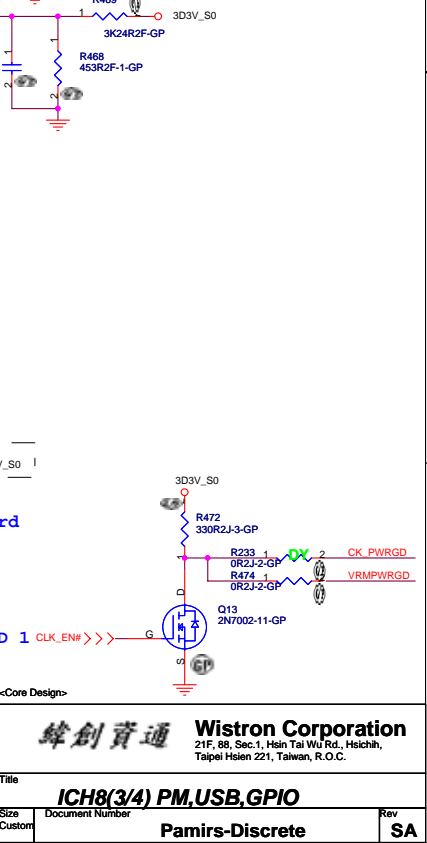
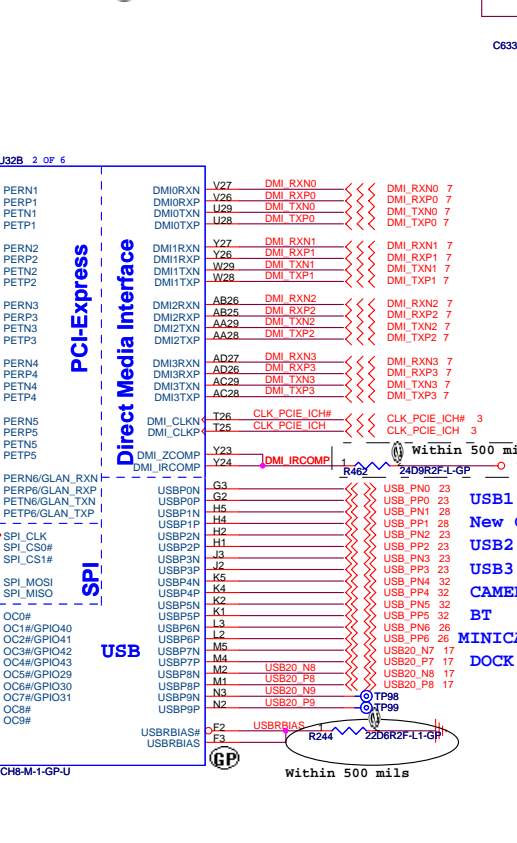
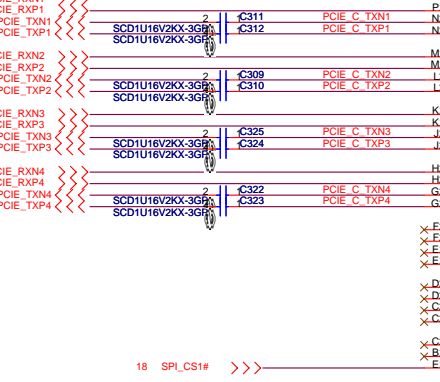
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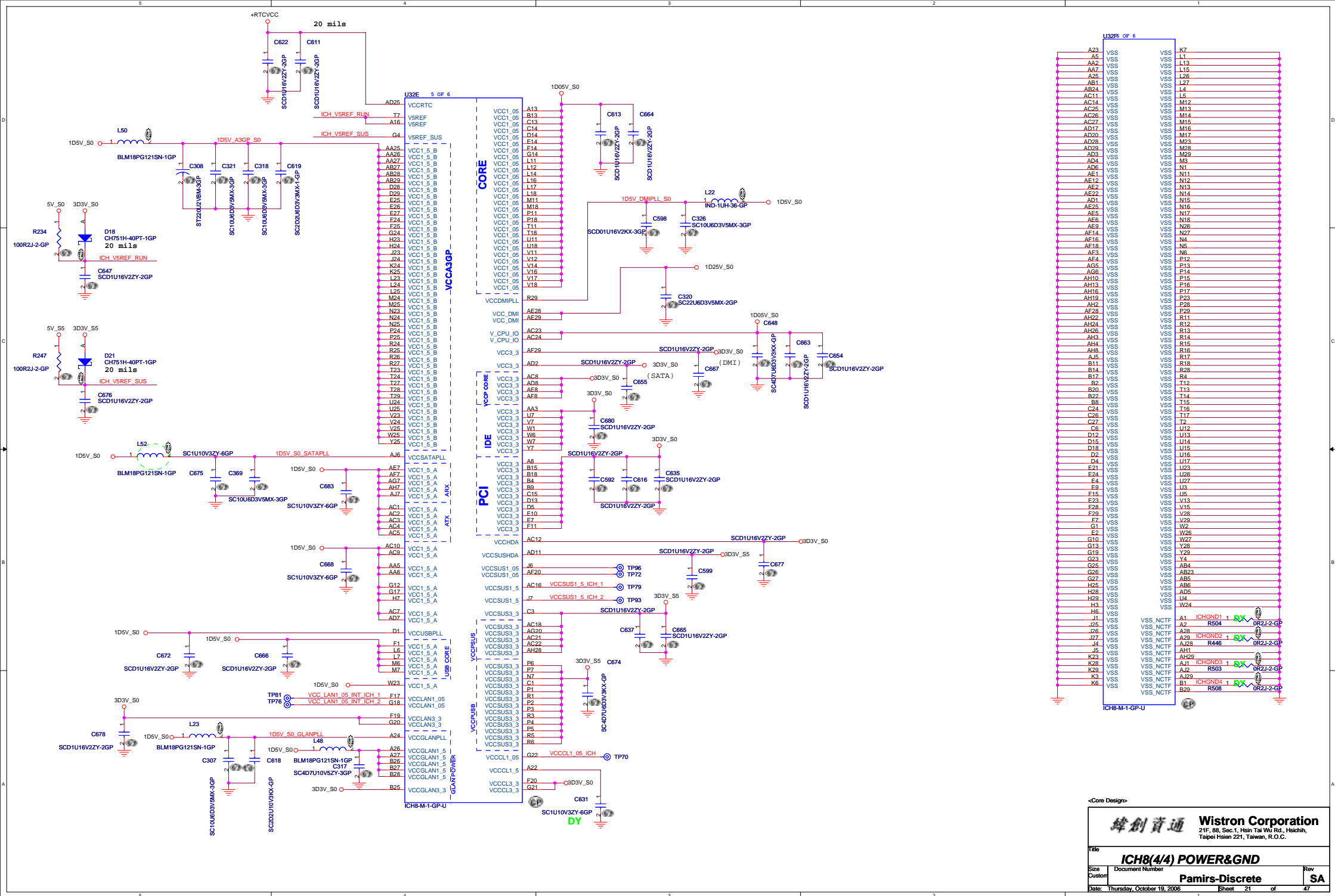


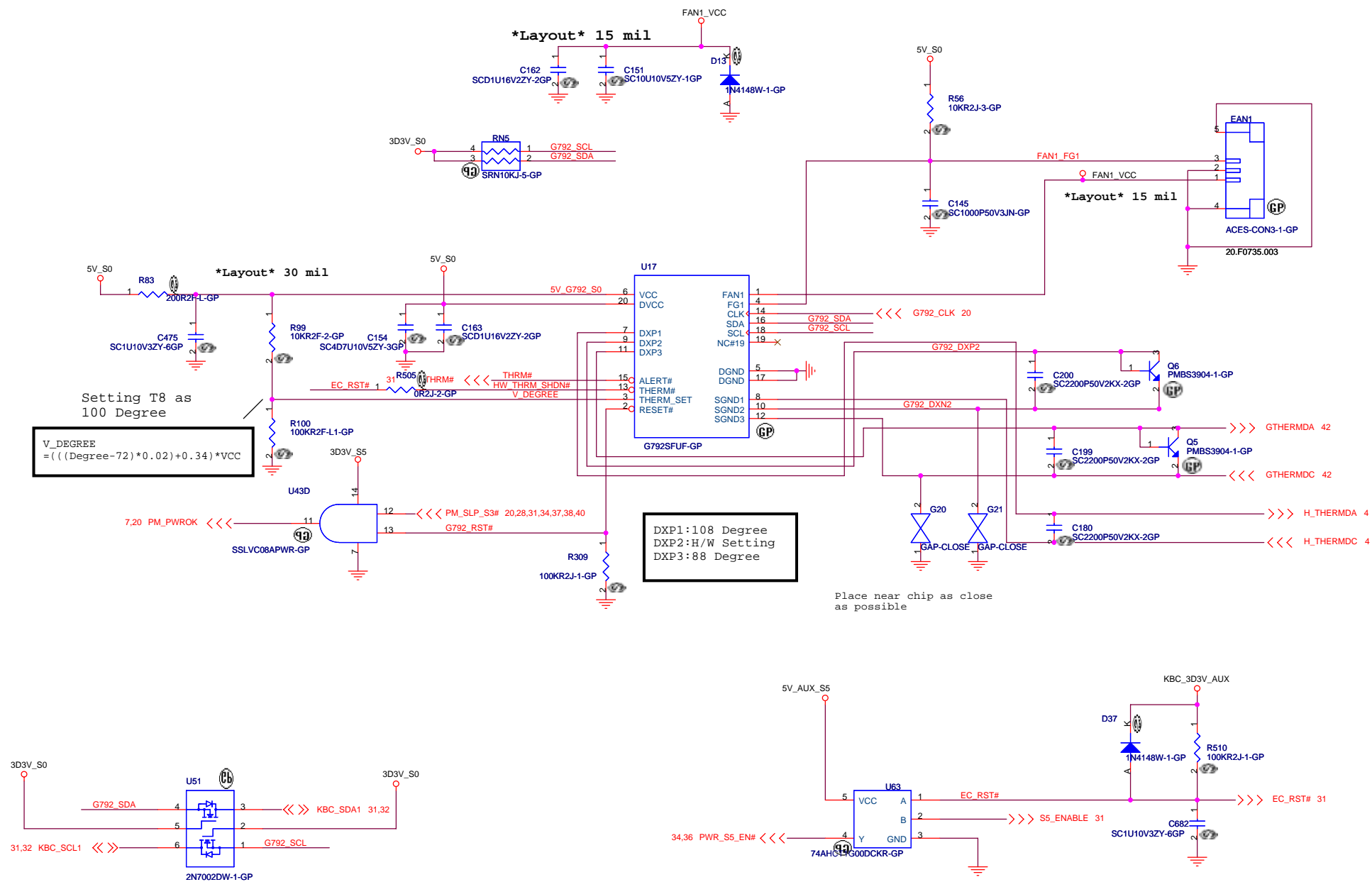


Low--> default
High--> No boot

Low--> default
High--> No boot





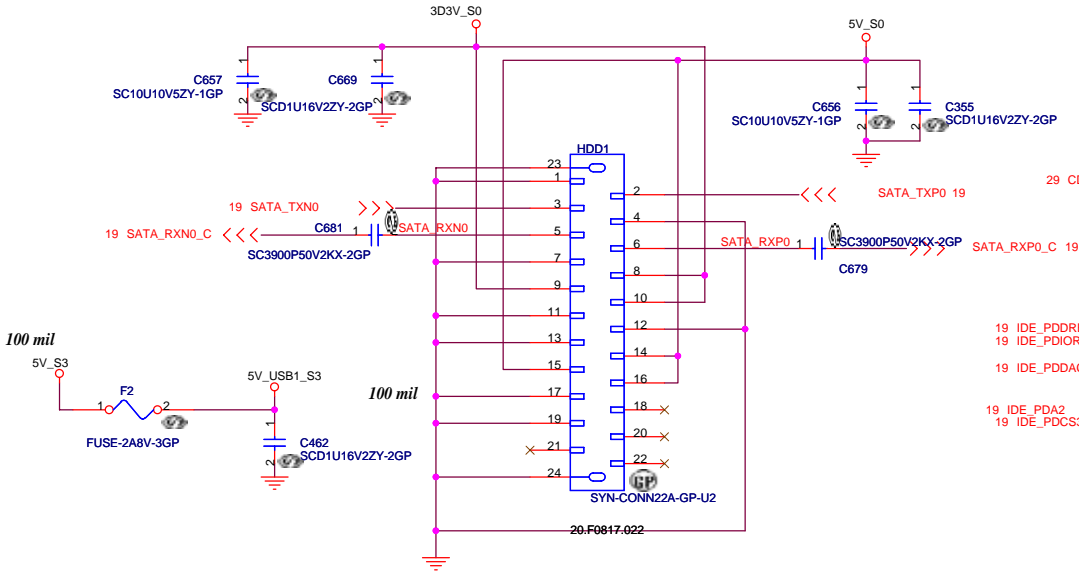


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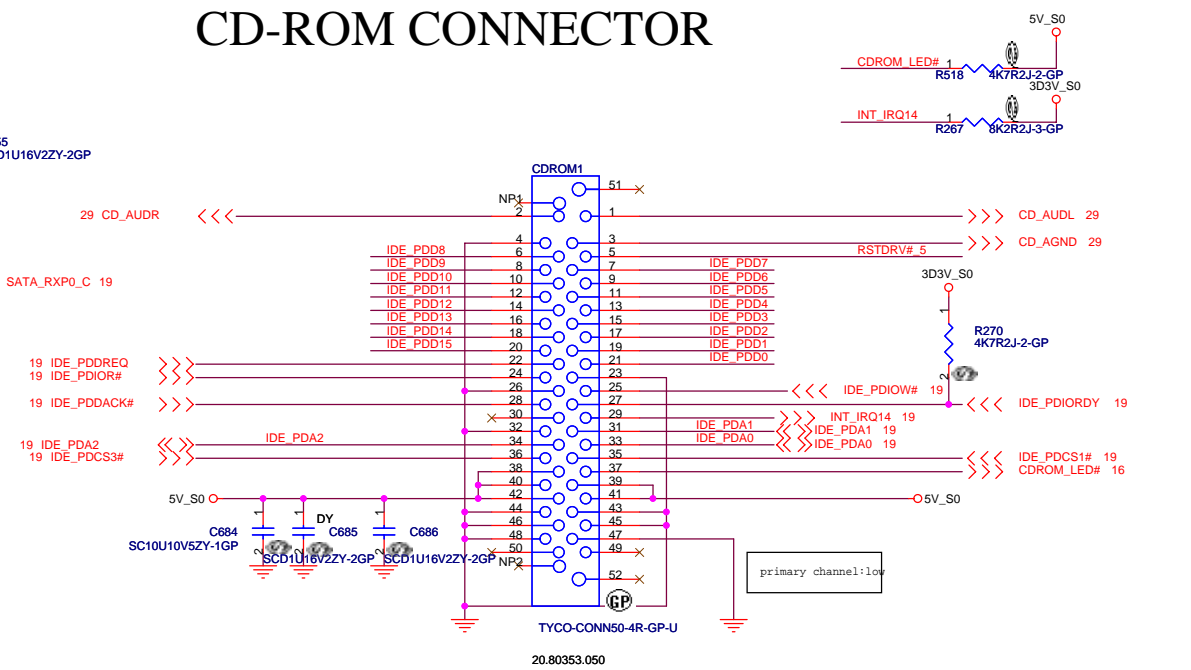
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Thermal/Fan Controller G792		
Size	Document Number	Rev
Custom	Pamirs-Discrete	SA
Date: Monday, October 23, 2006	Sheet 22 of 47	

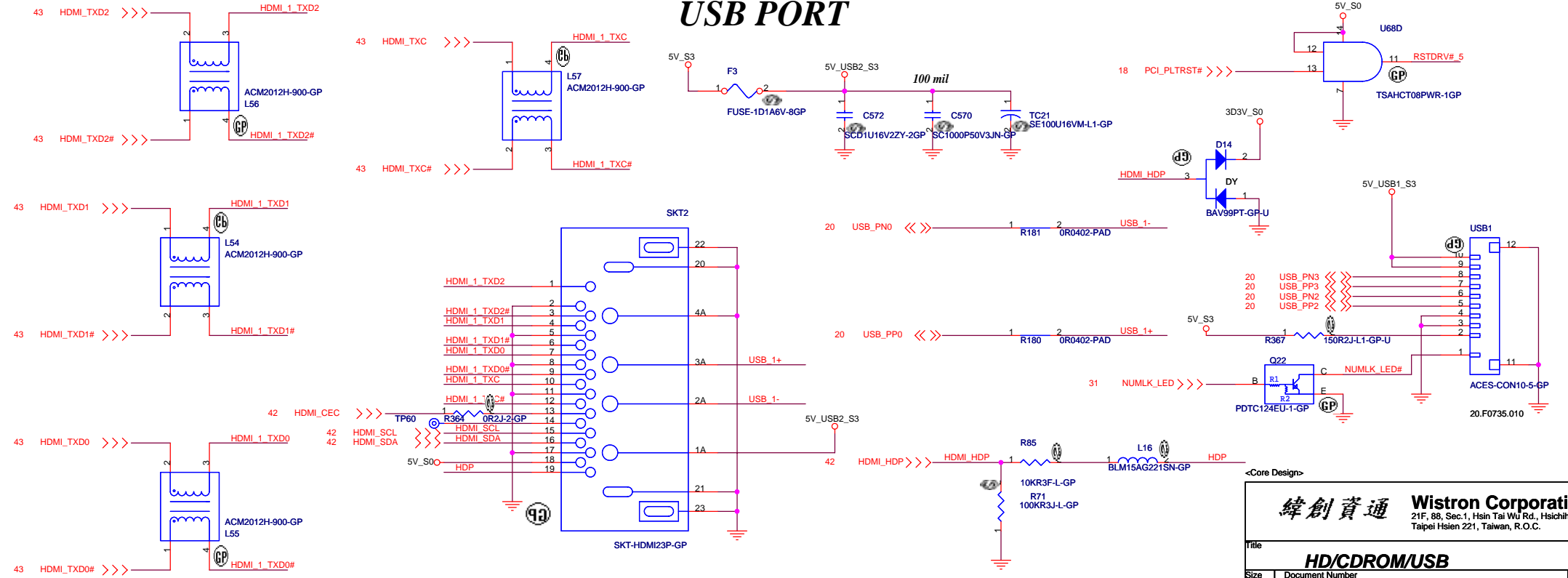
SATA HD Connector



CD-ROM CONNECTOR

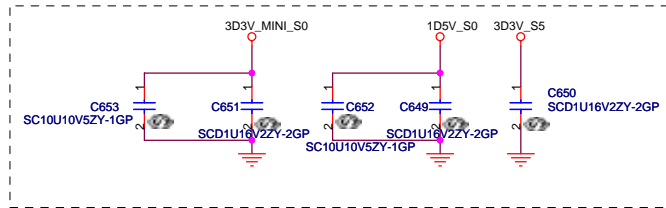
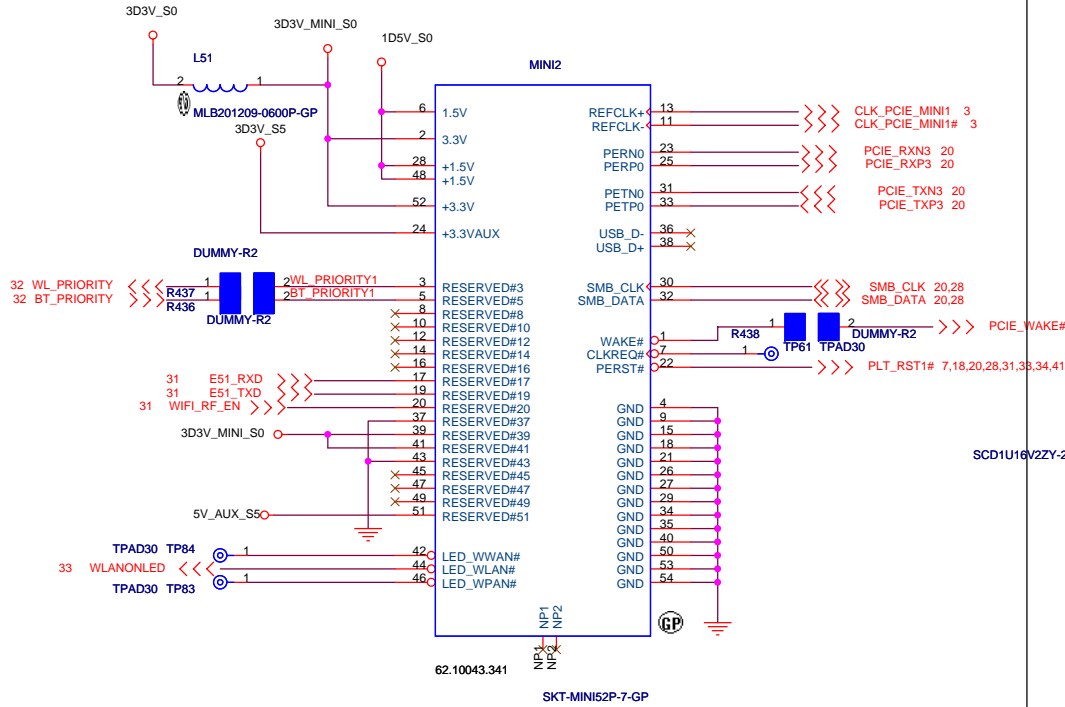


USB PORT



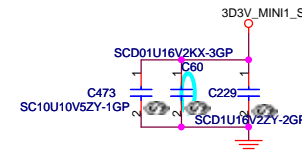
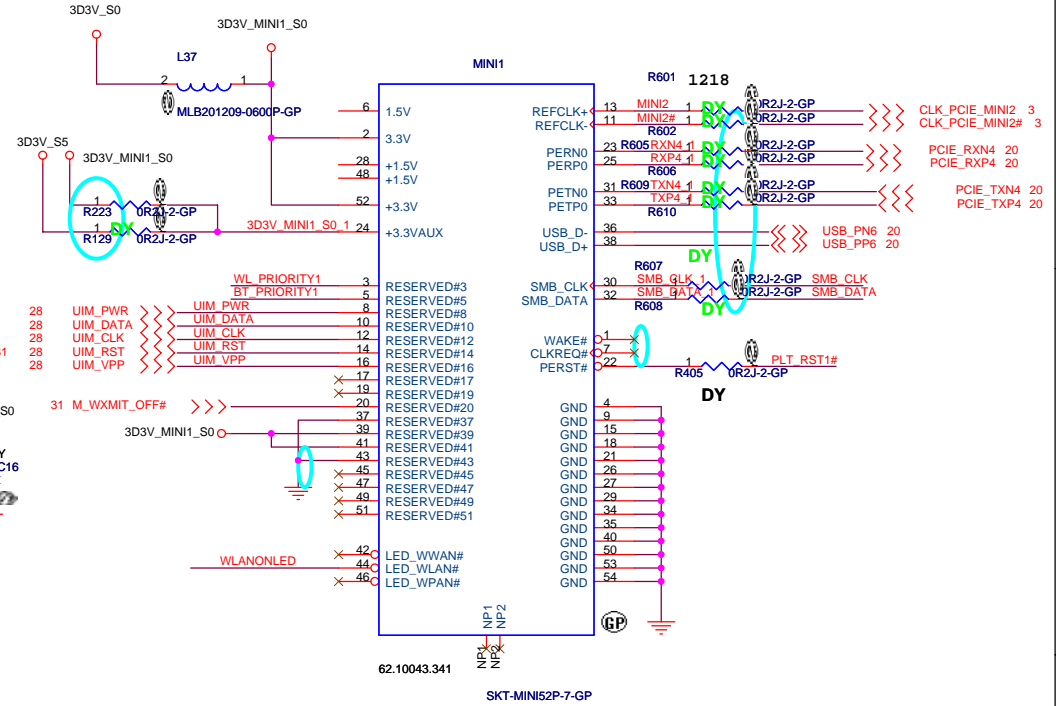
Mini Card Connector 2

Wireless card



Mini Card Connector 1

WWAN



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI CARD CONN.

Size
A3

Document Number

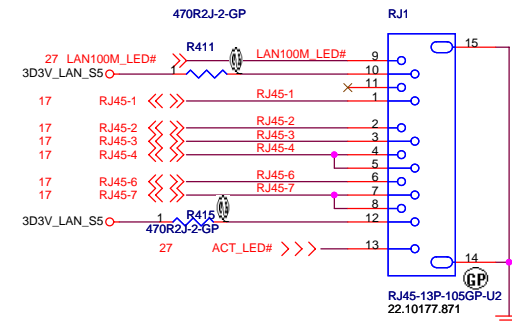
Pamirs-Discrete

Rev
SA

Date: Tuesday, December 19, 2006

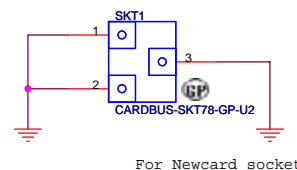
Sheet 26 of 47


```
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW
```

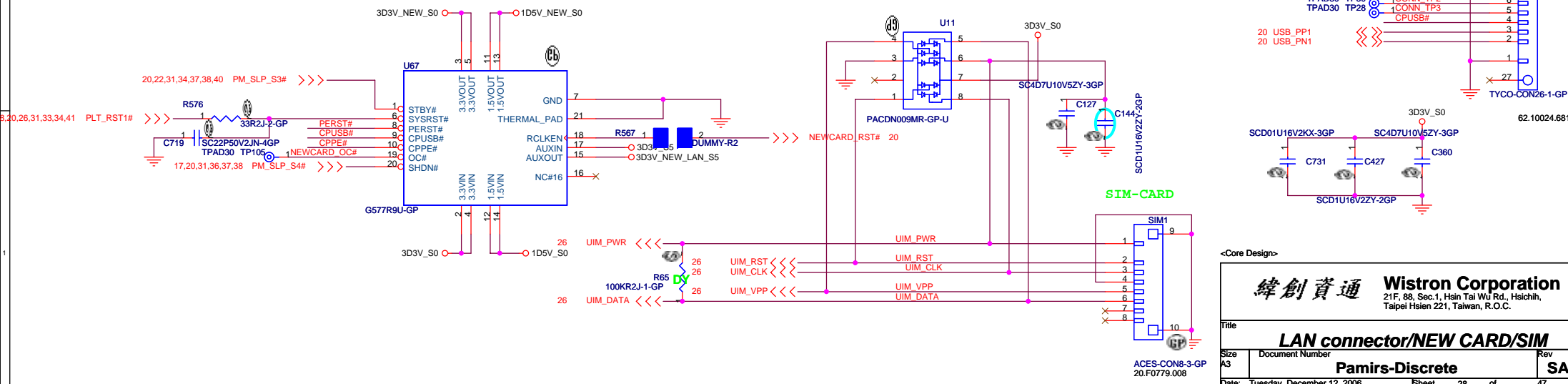


Green : Link up
Blinking : TX/RX activity

Place them Near to Connector



For Newcard socket



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN connector/NEW CARD/SIM

Size

Document Number

CONNECTOR/NEW

Rev

A3

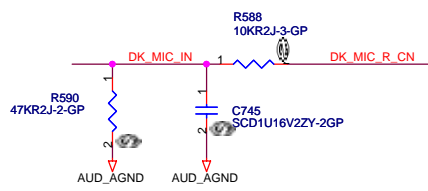
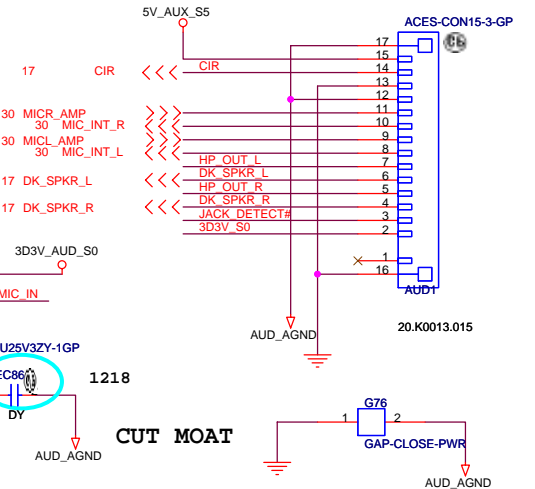
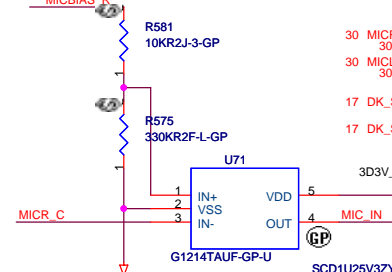
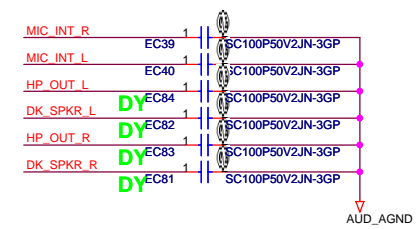
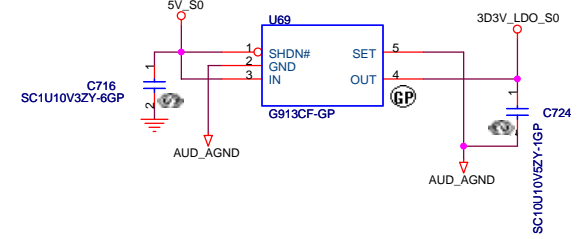
Pamirs-Discrete

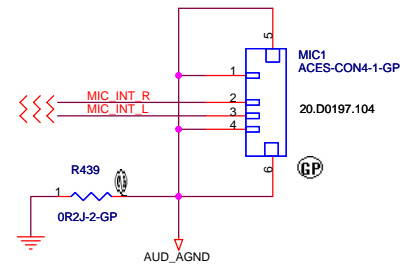
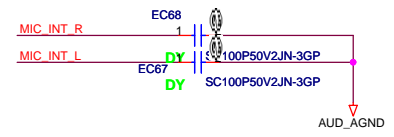
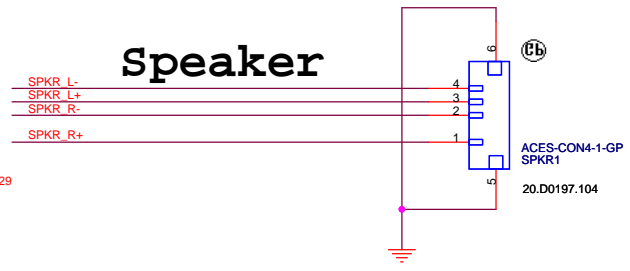
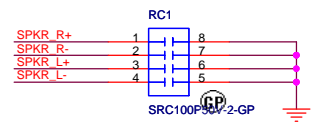
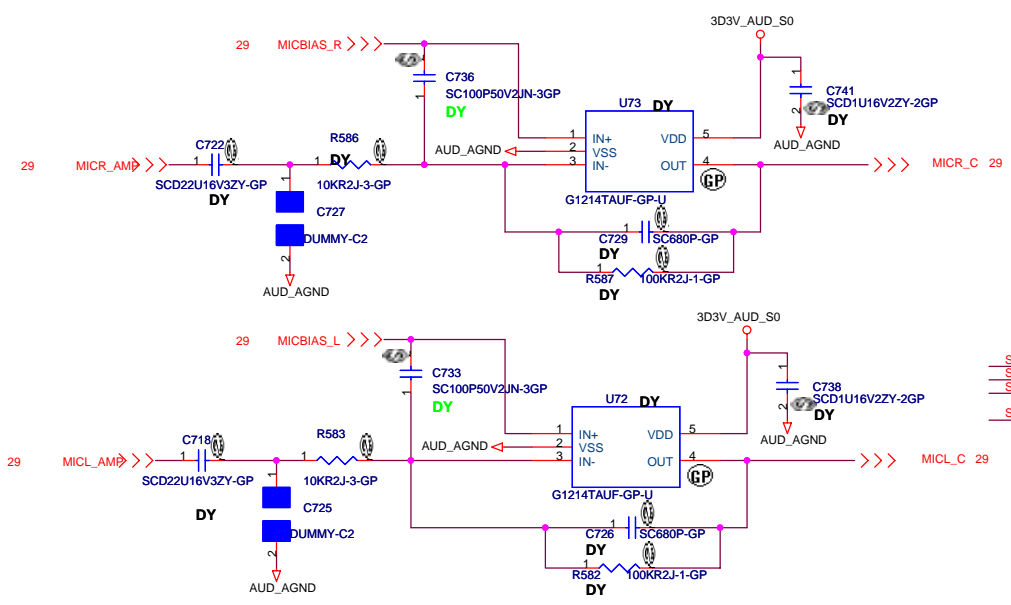
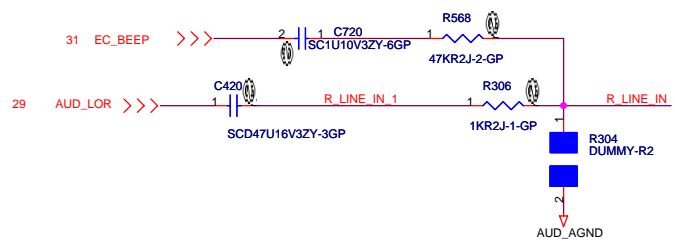
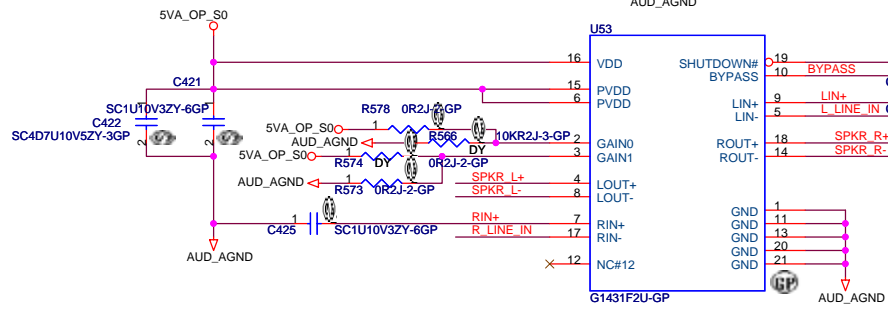
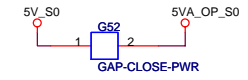
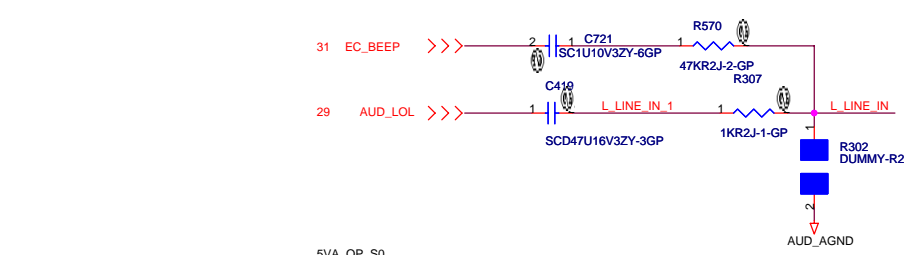
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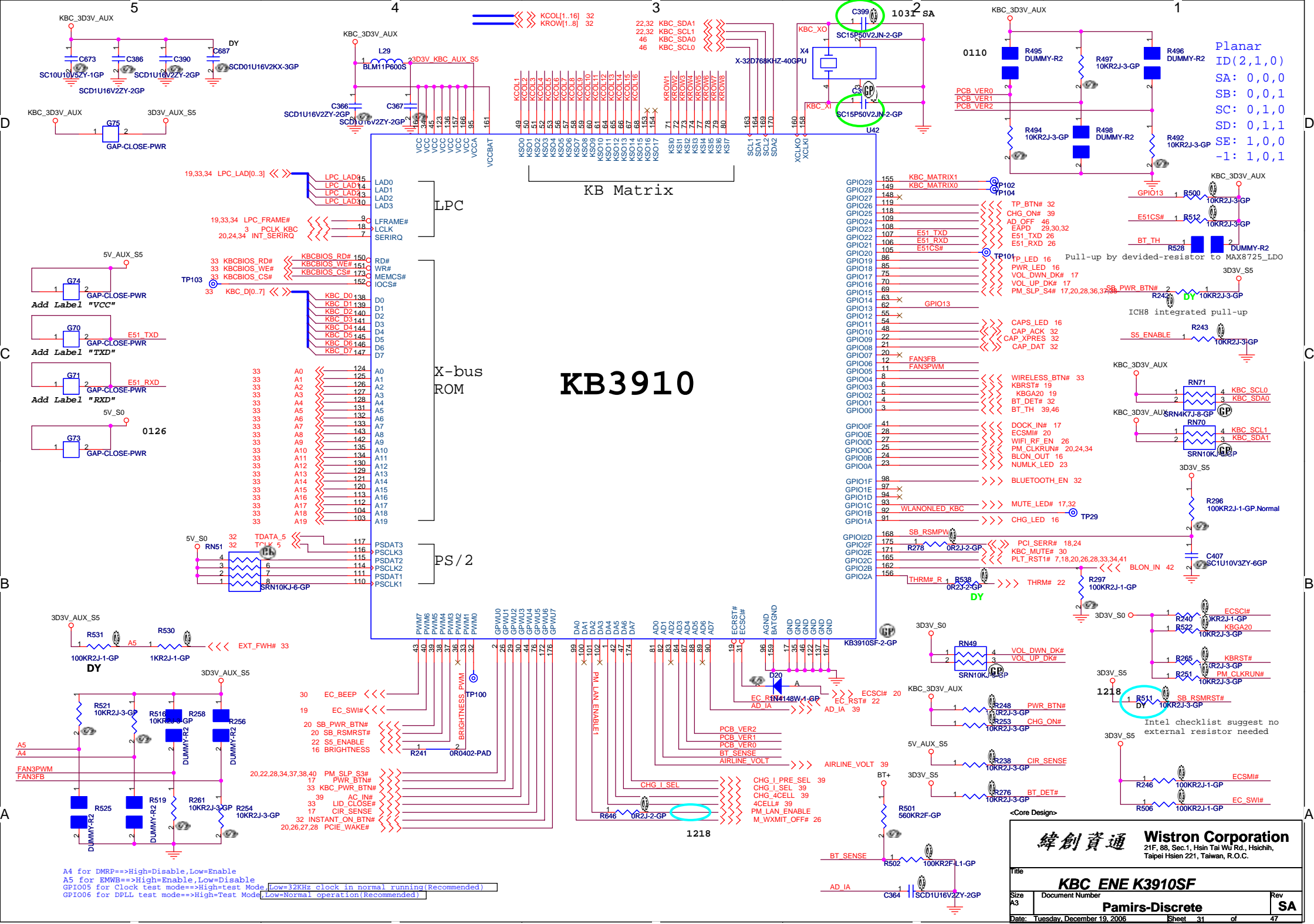
Date: Tuesday, December 12, 2006

Sheet

47







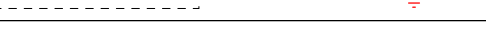
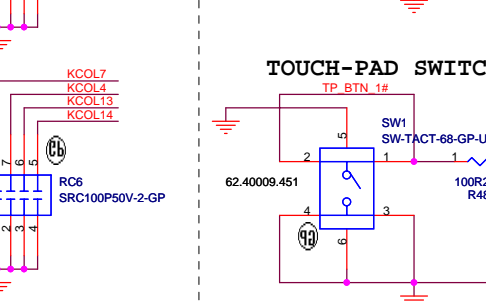
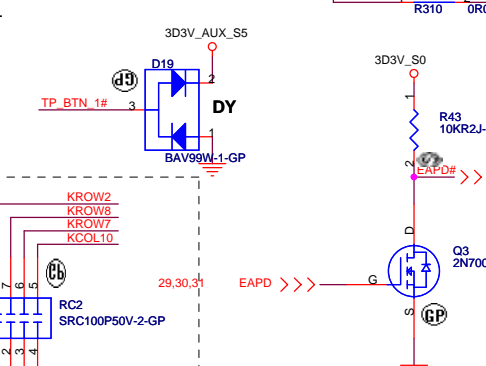
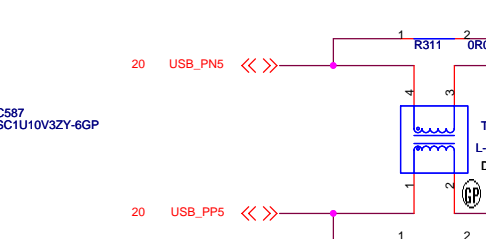
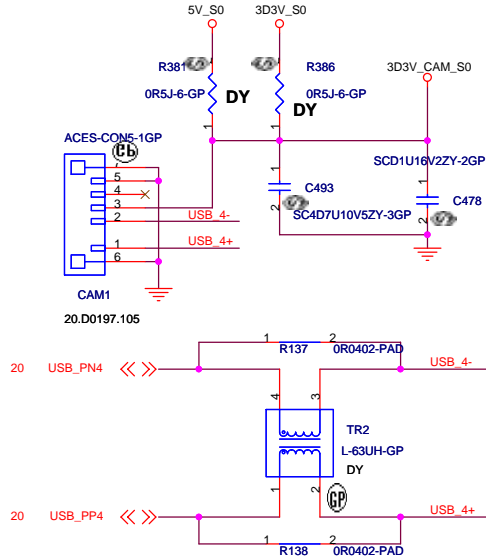
CAMERA

Internal KeyBoard Connector

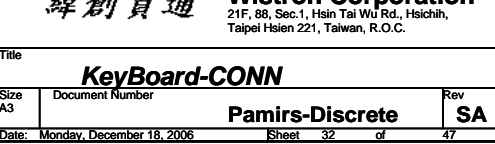
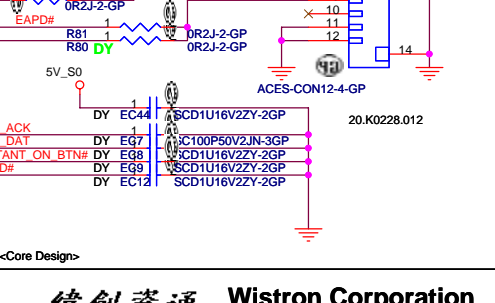
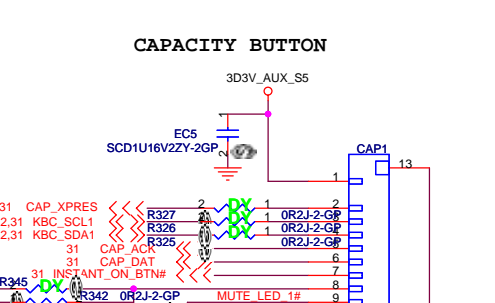
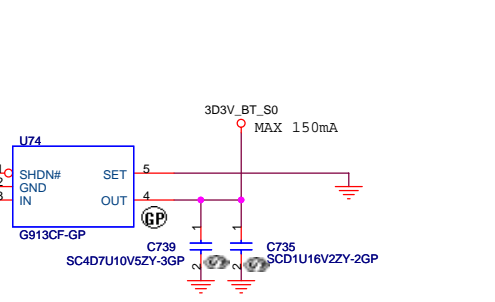
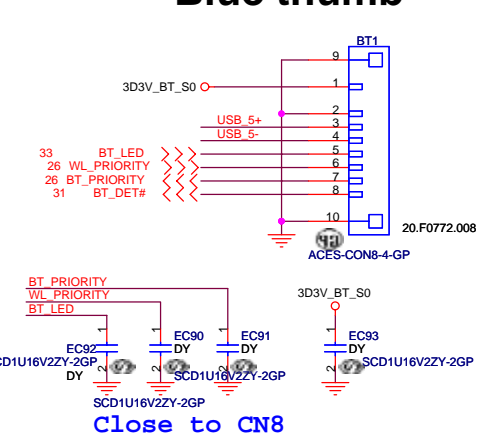
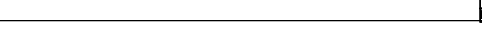
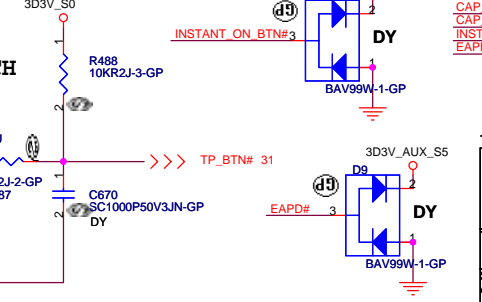
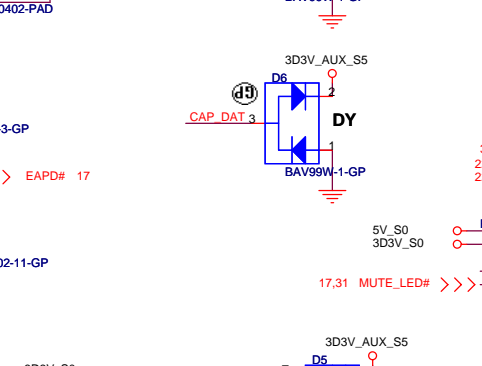
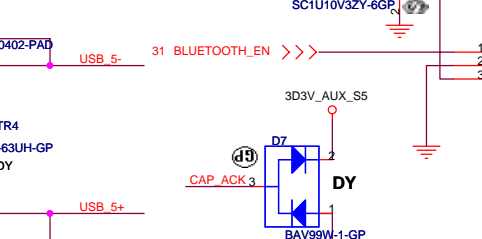
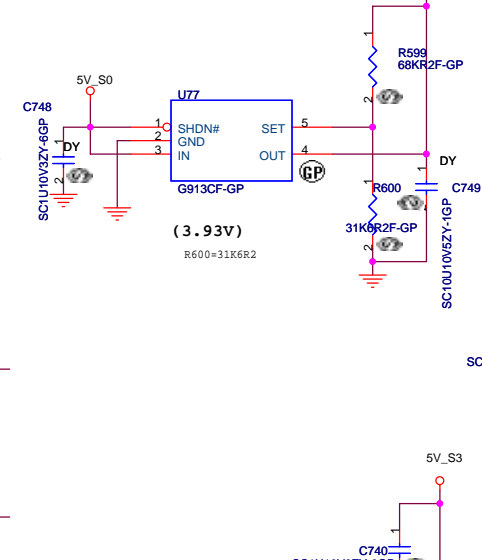
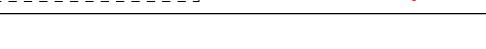
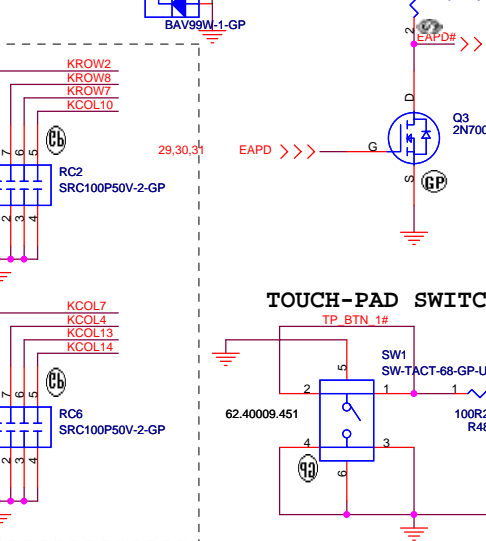
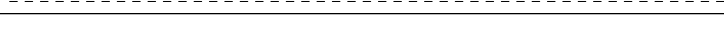
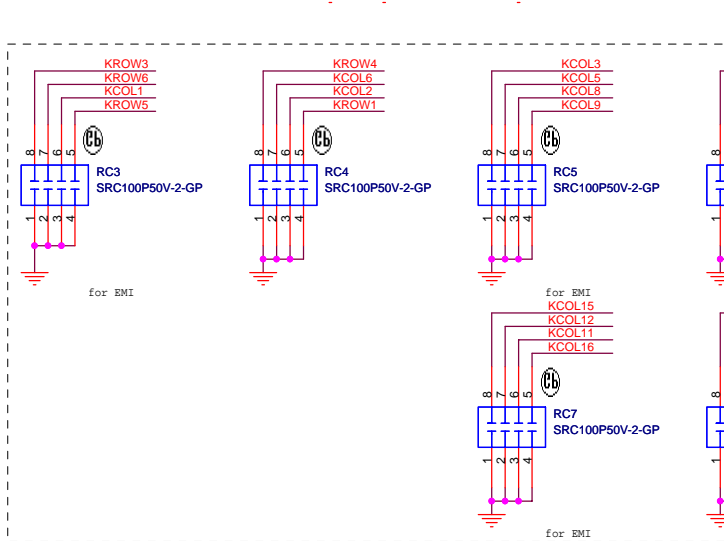
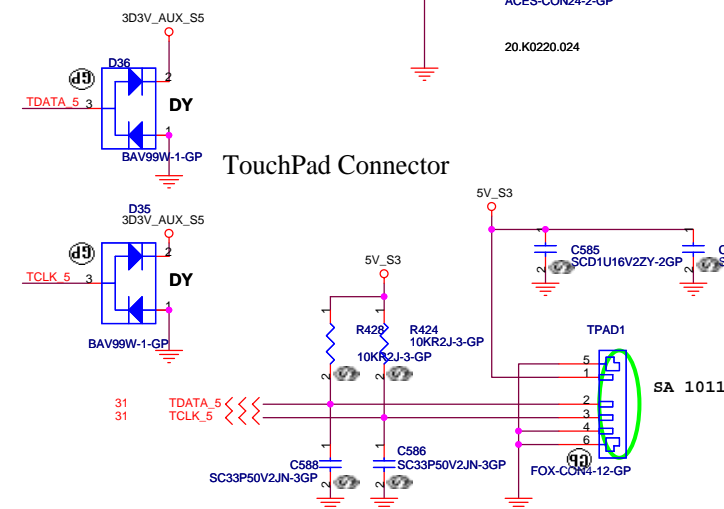
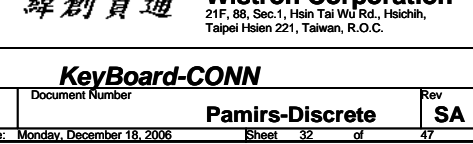
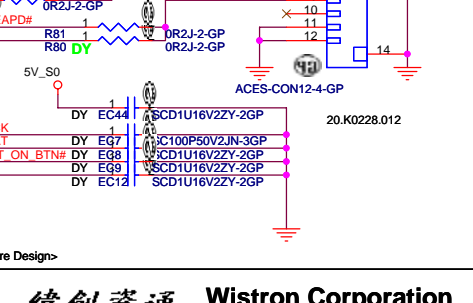
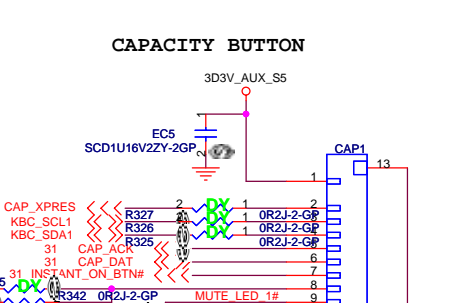
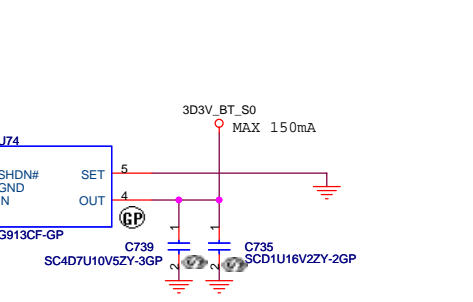
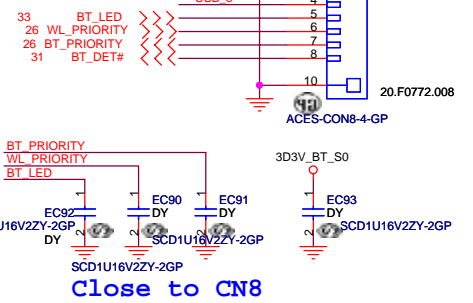
31 KROW[1..8] <<< <<<
31 KCOL[1..16] <<< <<<

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



Blue thumb



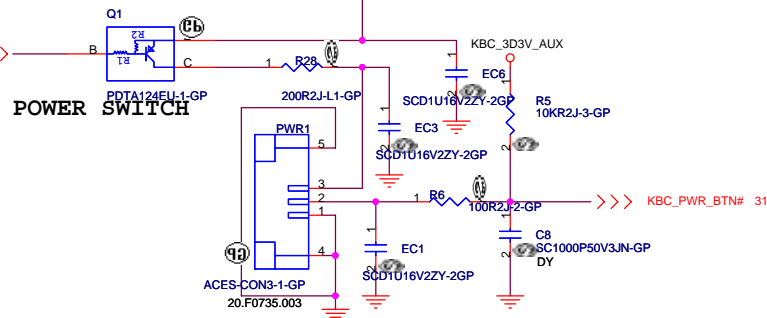
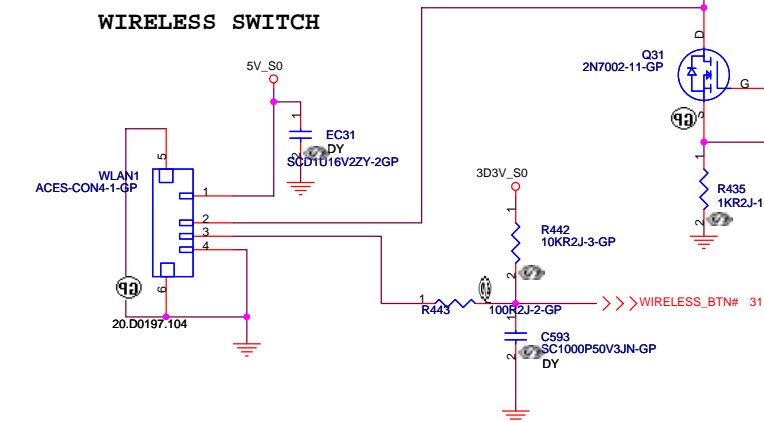
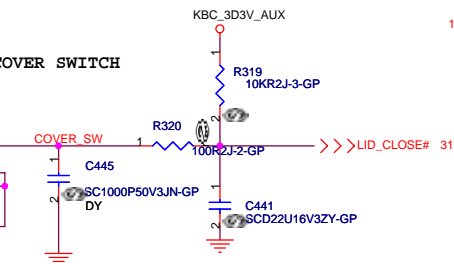
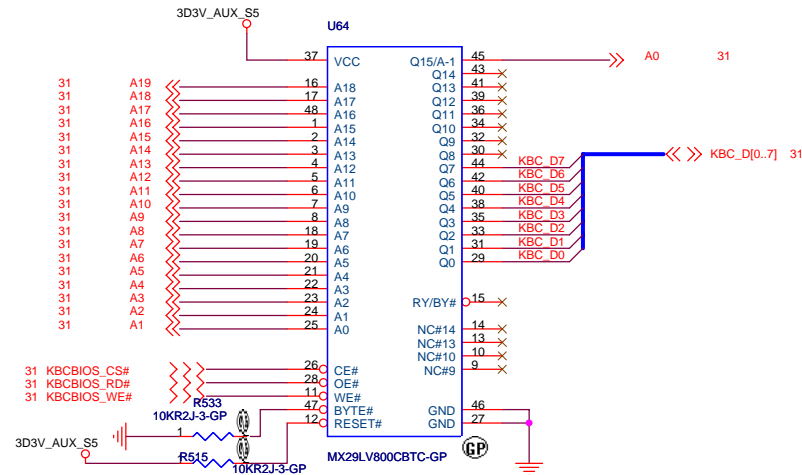
<Core Design>

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Title **KeyBoard-CONN**

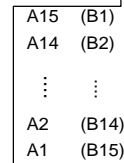
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POWER SWITCH

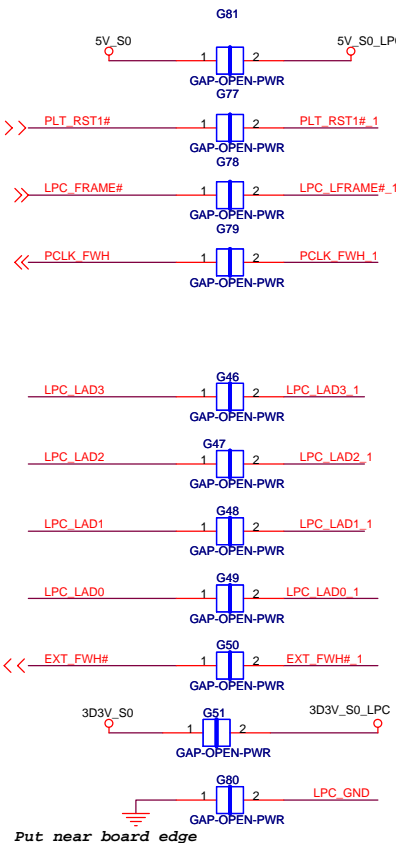
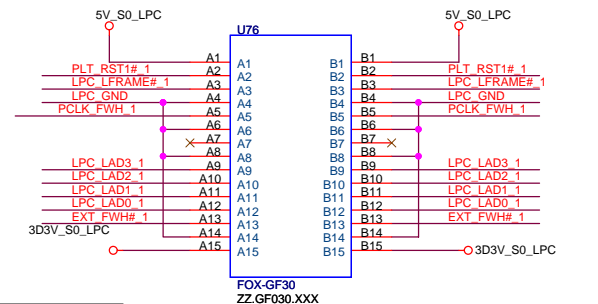
TOP VIEW



(BOTTOM VIEW)

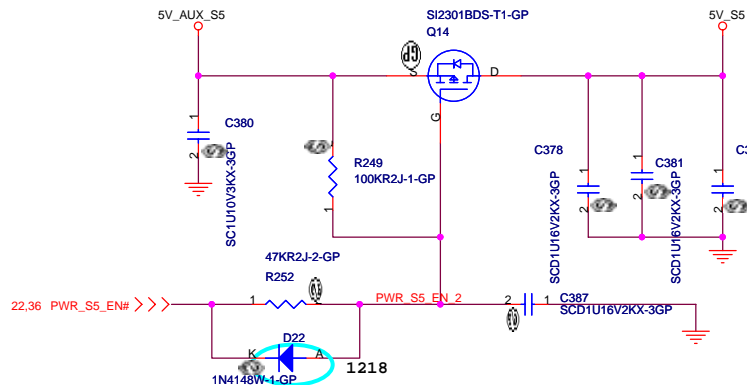
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

GOLDEN FINGER FOR DEBUG BOARD

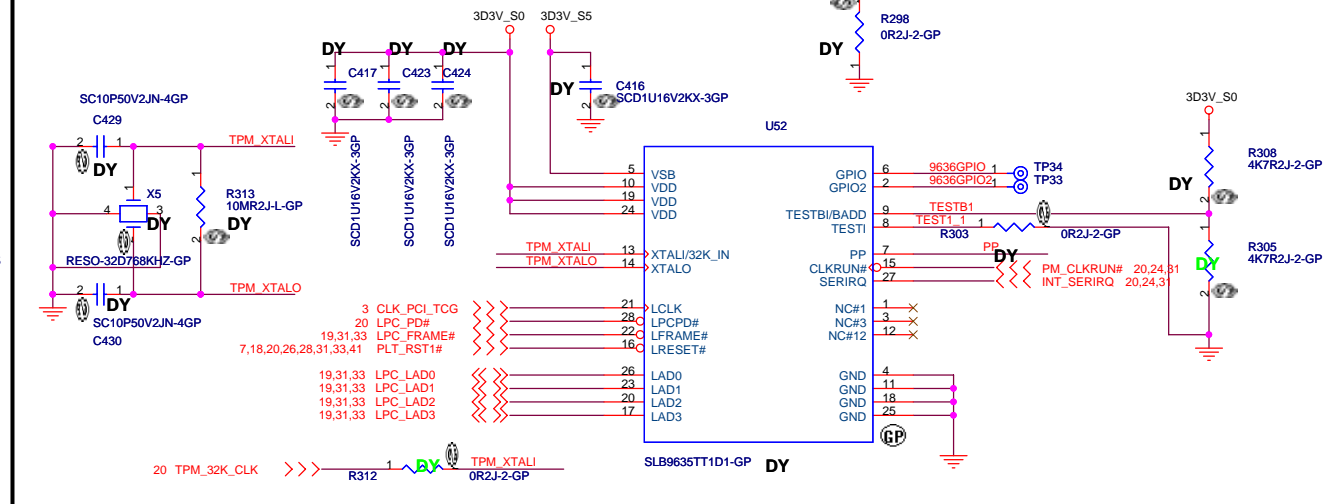


<Core Design>

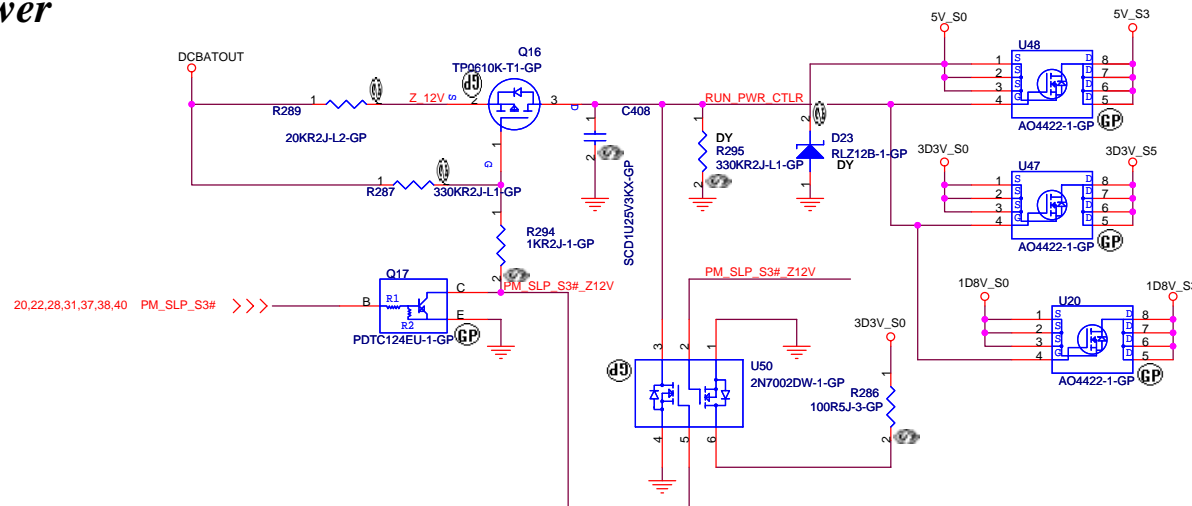
5V_AUX_S5 TO 5V_S5



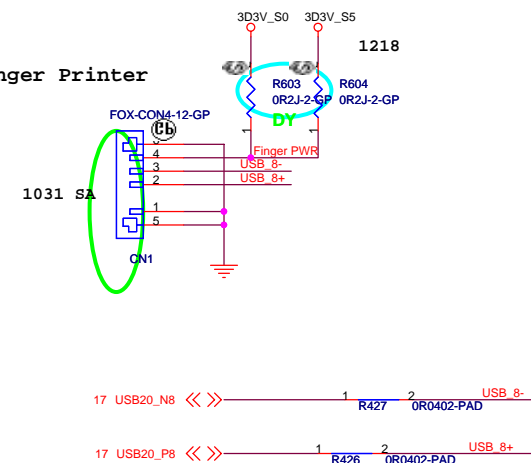
TPM 1.2



Run Power



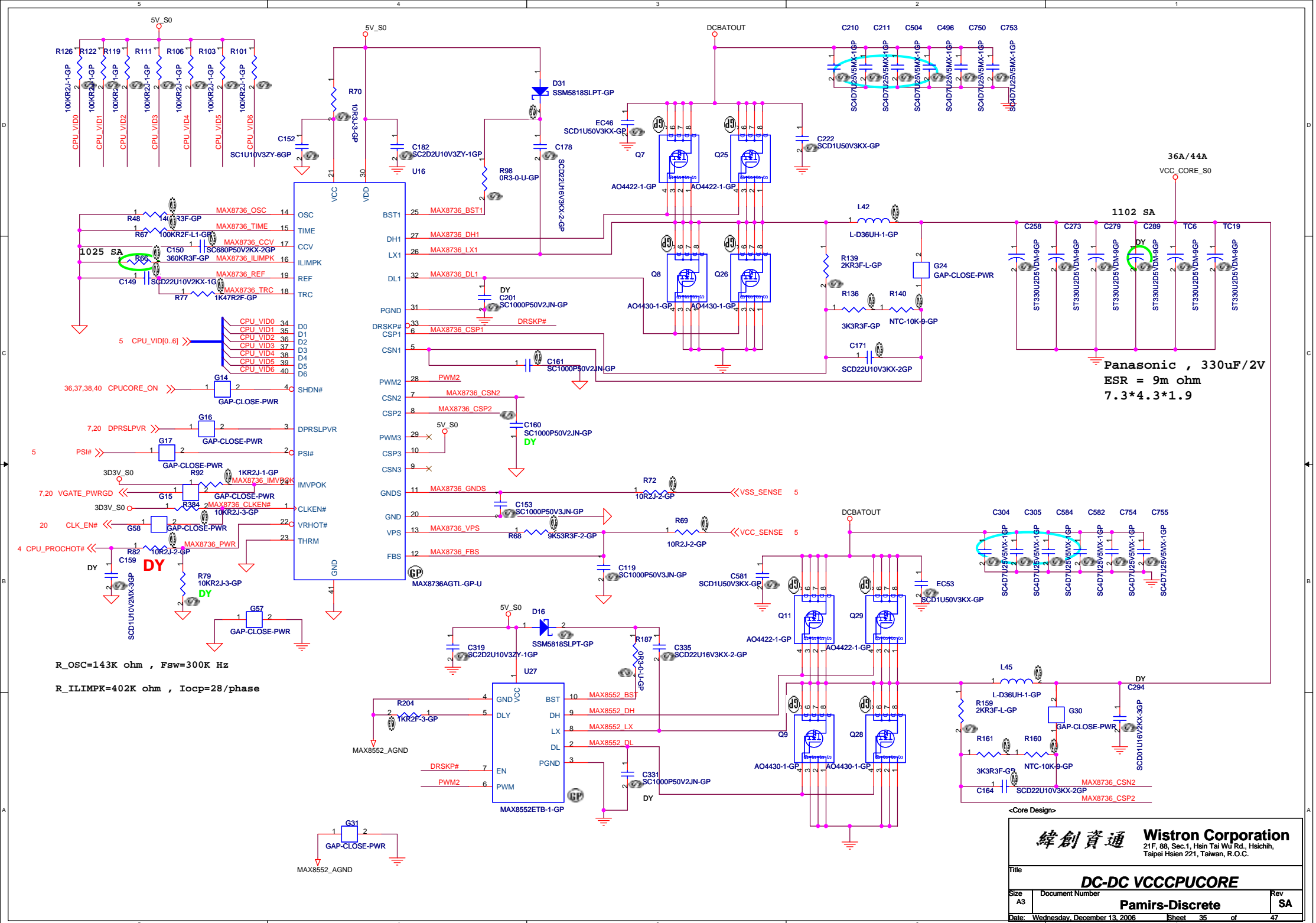
Finger Printer

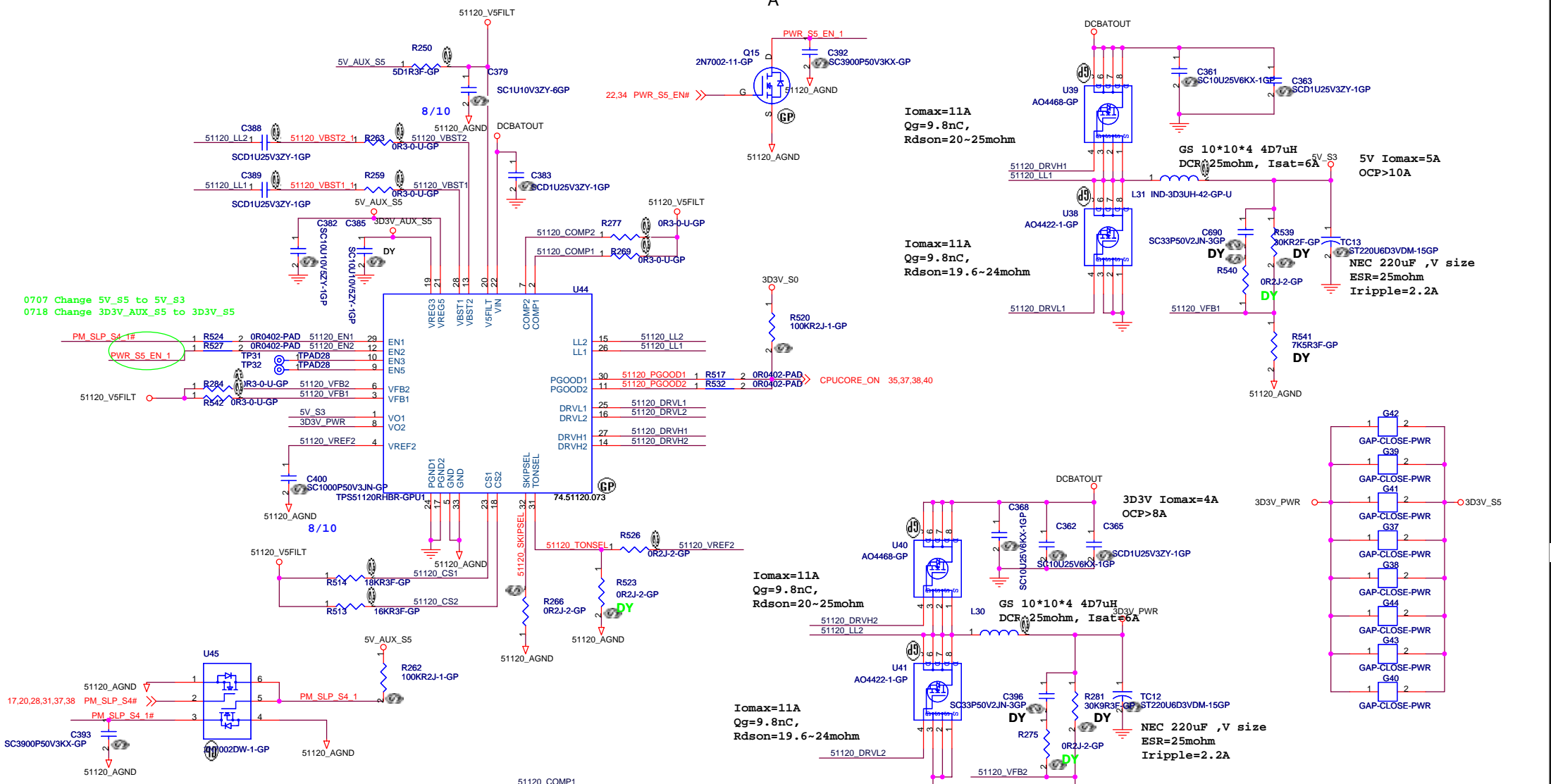


<Core Design>

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Title			
PWRPLANE&RESETLOGIC			
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	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

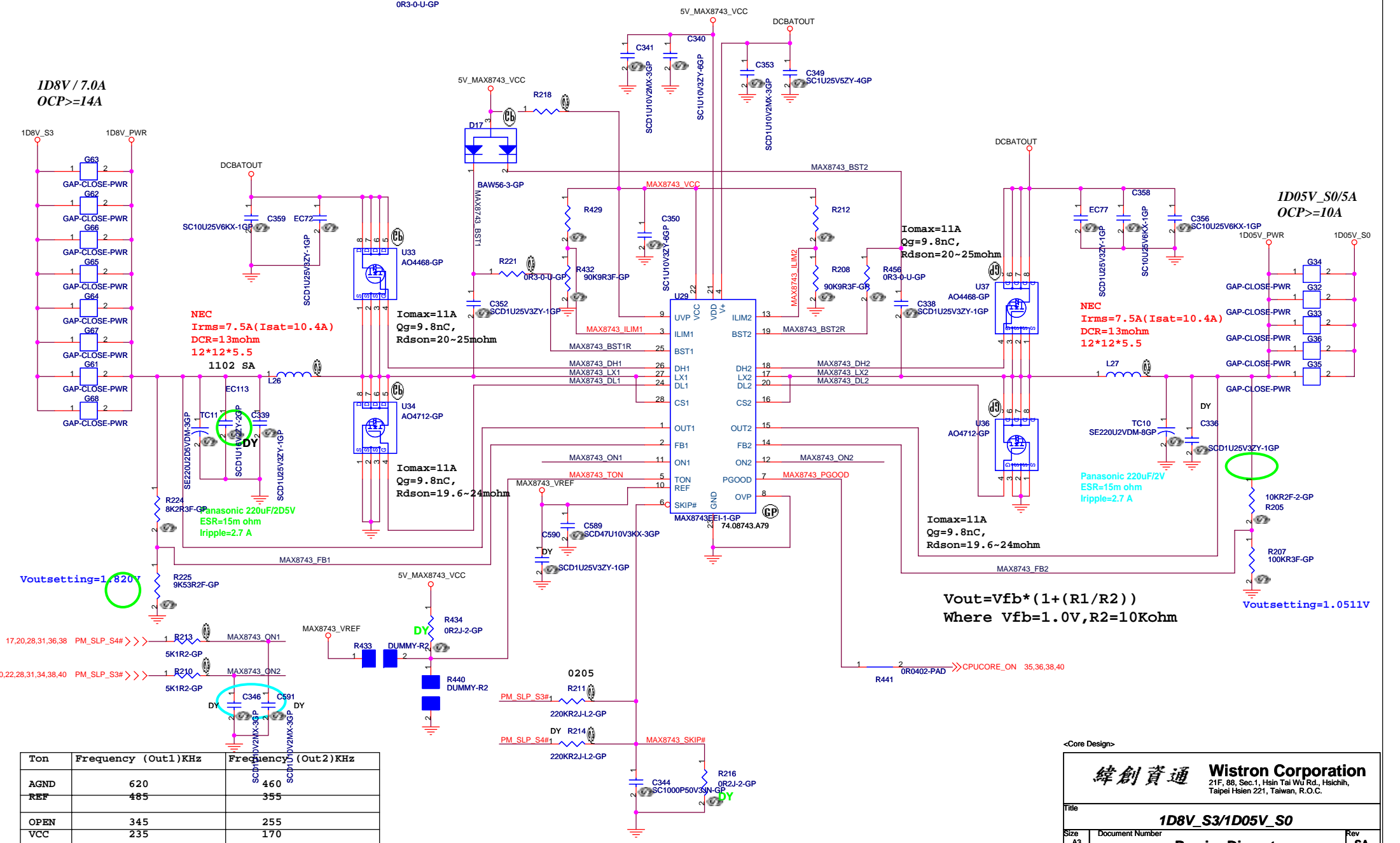
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Title: **5V_S3/3D3V_S5**

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$I_{ocp}=7.0*2=14A$
 $R_{ds,on}=17m\ ohm$
 $V_{cs1}=I_{ocp}*R_{ds,on}=238mV$
 $V_{ILIM}=V_{cs1}/0.1=2.38V$

$I_{ocp}=7.0*2=14A$
 $R_{ds,on}=17m\ ohm$
 $V_{cs2}=I_{ocp}*R_{ds,on}=28mV$
 $V_{ILIM2}=V_{cs2}/0.1=2.38V$



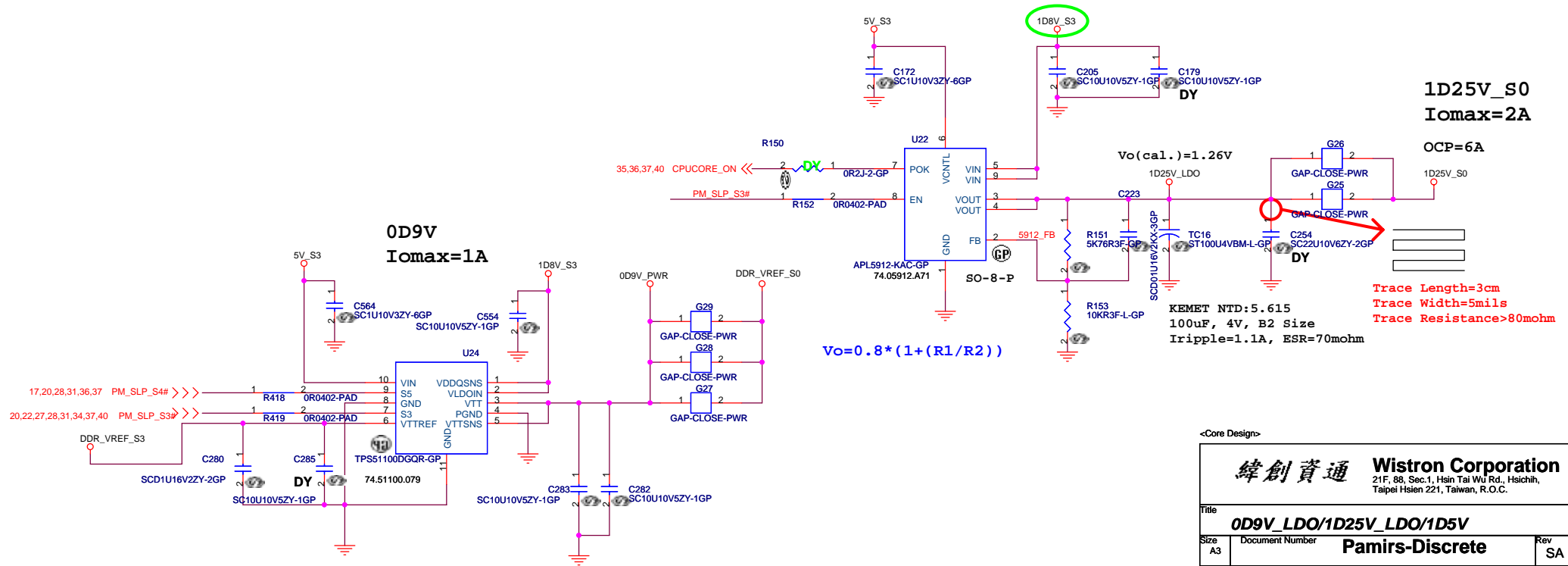
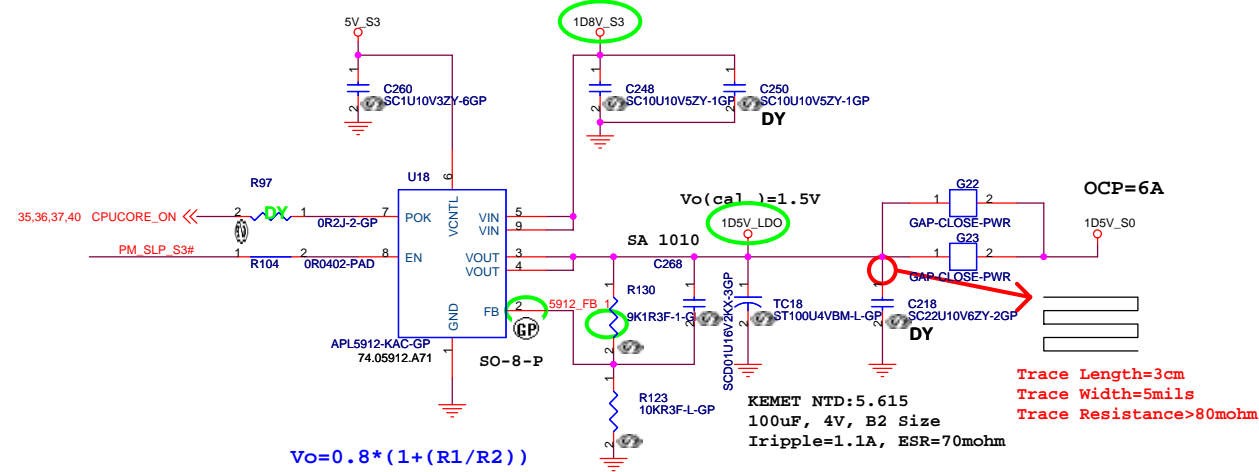
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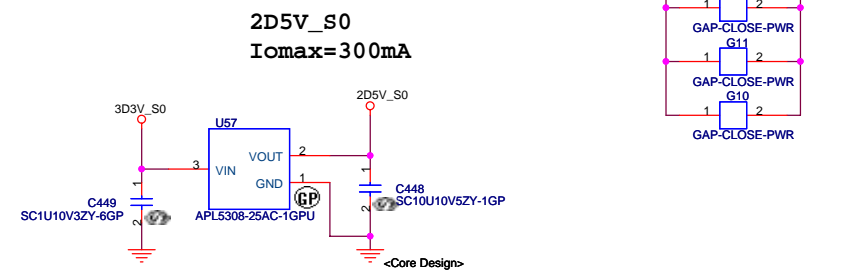
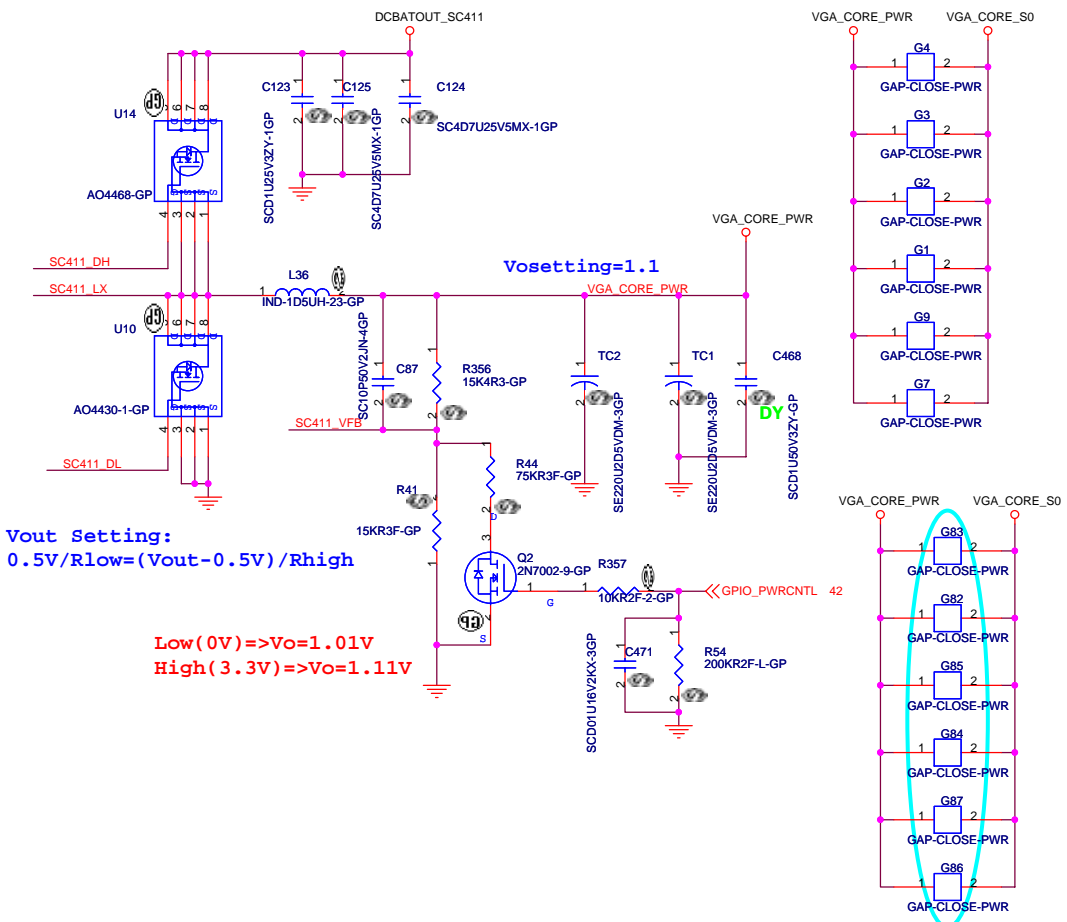
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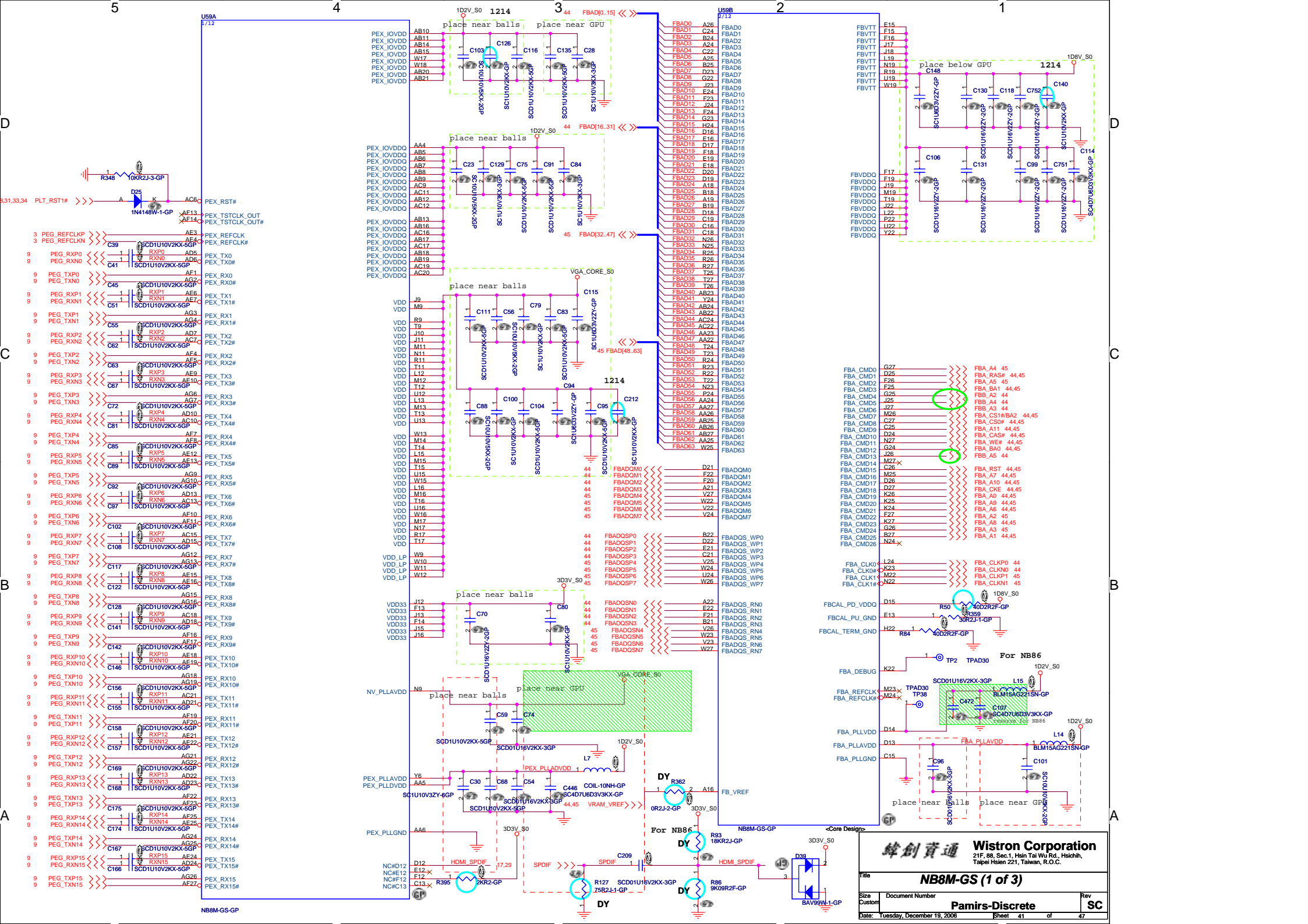
Title: **1D8V_S3/1D05V_S0**

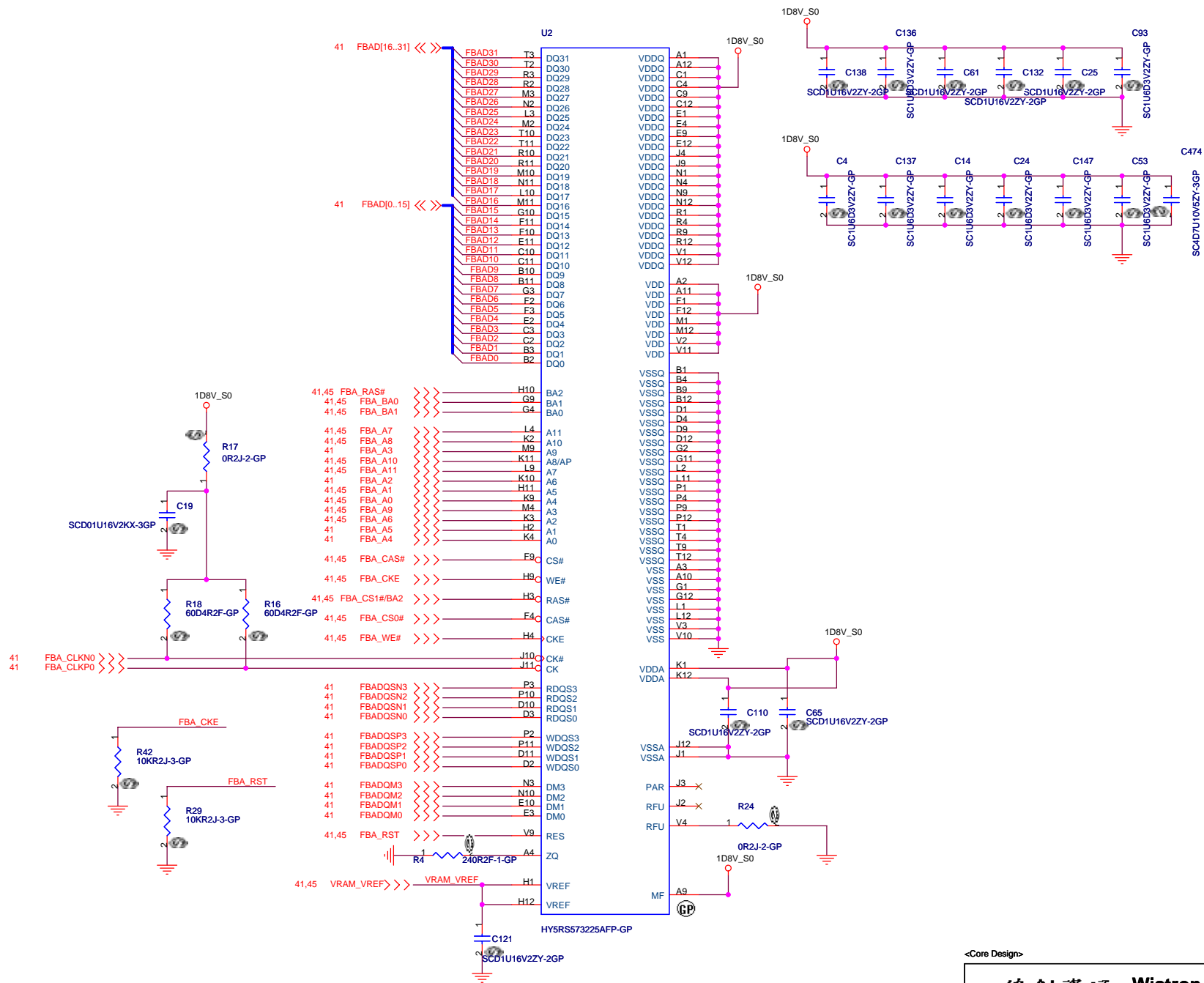
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Title			
AD/BATT CONN			
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